CMOS Analog IC Design [2018-19]

Assignment 2 [50 Marks]

Deadline: 6th September 2018 - 11:55 PM

Common instructions:

- **For all the questions take $V_{DD} = 1.8V$, $L = 0.18\mu m$ and unit Finger Width of $0.5\mu m$ unless mentioned otherwise**
- **All NMOS bodies must be connected to GND and PMOS bodies to VDD but ignore body effect in all hand calculations**
- **Show the formula for necessary variables (like gain, input impedance, output impedance etc.) and explicitly mention how you designed the circuit to meet the given specifications.**
- **Simulation results without explanations/design steps don't carry any marks.**
- **Please show the cadence circuit schematic (with all component values visible), your results, waveforms or explanations in a clear and understandable manner.**
- **For all questions, try to start from simple expressions for gain, input impedance, output impedance etc., and later iterate the design (if needed) by including other terms.**
- **In the waveforms, highlight important points using markers.**
- **Bandwidth in the scope of the assignment always refers to the 3dB Bandwidth and Slew Rate refers to the output Slew Rate**
- **All the answers must contain units.**

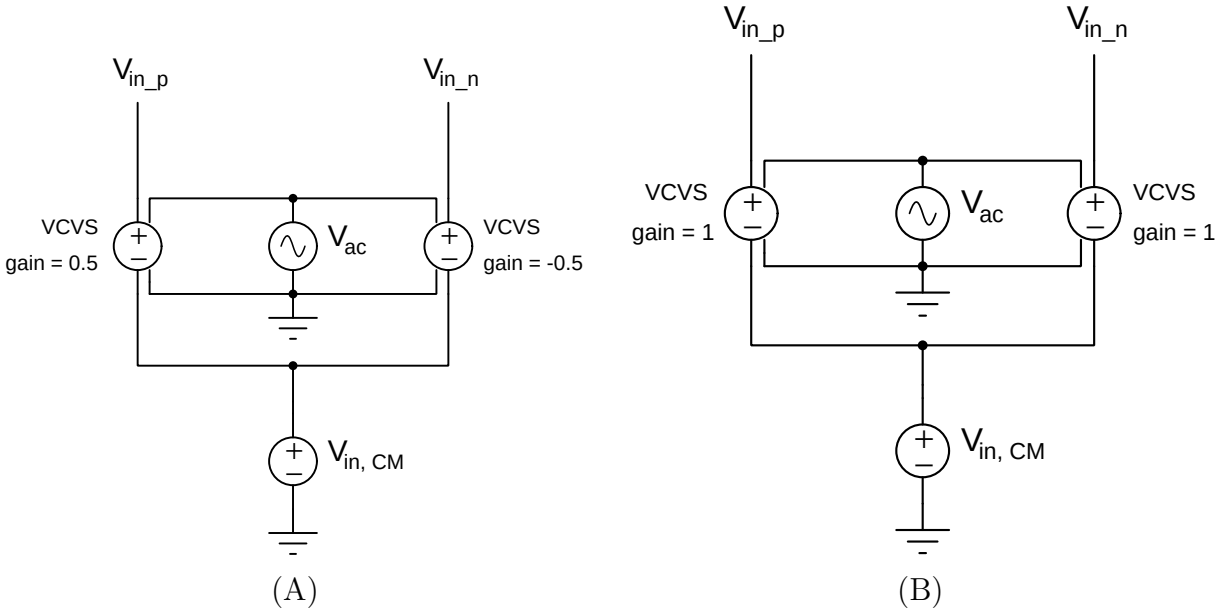

Figure 1: (A) Differential Input Setup (B) Common Mode Input Setup

Question 1

Part A

To start off, you will be designing a simple differential amplifier with diode connected load as shown in Figure 2 below. Your design should meet the following specifications.

Parameter	Value
Gain	>11 dB
$V_{in,CM}$	1.1V
$V_{out,CM}$	0.9 V ($\pm$10%)
DC Power	<60 μW
Current Source Headroom	>0.5V

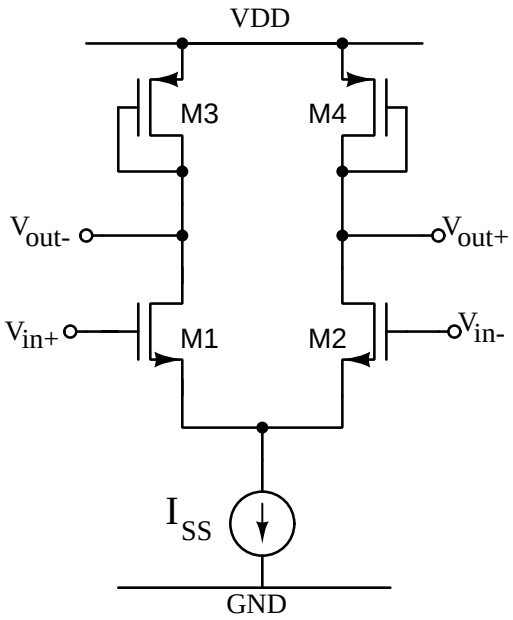

Figure 2: Differential Amplifier with Diode Load

- Derive the expression for the DC gain (differential gain) of the circuit as a function of g_m and g_{ds} of the transistors [1 Mark(s)]
- Show the step-by-step design procedure and iterate on the design to meet the specifications in the simulation. Tabulate the final values of the W of the transistors and I_{SS} [2 Mark(s)]
- Show the schematic of the circuit with DC Operating points annotated clearly [1 Mark(s)]
- Perform a transient analysis using the differential mode setup with a 10mV sinusoidal input at 10KHz. Plot the input and the output waveforms and clearly mark the peak values in the plot [1 Mark(s)]
- Perform ac analysis using the differential mode setup and clearly indicate (through markers/cursors) the dc gain [1 Mark(s)]
- Tabulate all the parameter values obtained by simulation as follows. [1 Mark(s)]

Parameter	Value
Gain	
$V_{out,CM}$	
DC Power Consumption	

Part B

In this part, you will be designing the tail current source for the differential amplifier you designed in Part A. For this you will be using a simple current mirror circuit as shown in Figure 3 below, keeping the current through M6 same as in Part A i.e. I_{SS}. Use the same design from Part A for transistors M1 through M4. Use I_B= 10 μA.

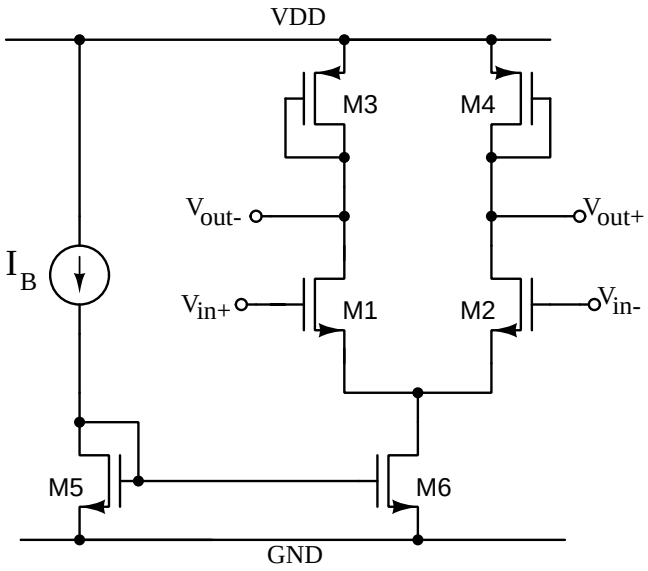

Figure 3: Differential Amplifier with Bias Current Mirror

- Briefly show design procedure and iterate on the design to meet the specifications in the simulation. Tabulate the final values of the width of the transistors M5 and M6 [2 Mark(s)]
- Show the schematic of the circuit with DC Operating points annotated clearly [1 Mark(s)]
- Perform a transient analysis using the differential mode setup with a 10mV sinusoidal input at 10KHz. Plot the input and the output waveforms and clearly mark the peak values on the plot. [1 Mark(s)]
- Perform ac analysis using the differential mode setup and clearly indicate (through markers/cursors) the dc gain [1 Mark(s)]
- **Noise Summary:**[1] Bandwidth of interest is 10KHz to 10MHz [4 Mark(s)]
  - Tabulate the input referred noise summary upto top 10 contributors by measuring the noise values at the output in a single ended manner (i.e. at V_{out+} w.r.t ground). Which is the major contributor to noise in this case?
  - Tabulate the input referred noise summary upto top 10 contributors by measuring the noise values at the output in a differential ended manner (i.e. $V_{out+} - V_{out-}$). Which is the major contributor to noise in this case?

P.T.O

[1]Refer to the uploaded document for details on simulating and performing noise analysis in virtuoso (Use the Integrated Noise Calculation section of the presentation). Apply only the DC Common Mode voltage while obtaining noise. This part can be completed after the lecture on Noise.

Question 2

Part A

Taking off from the previous question, here you'll be designing a simple fully-differential input and single-ended output OTA. Without altering the differential amplifier designed earlier, design the differential to single-ended converter for the following overall specifications:

Parameter	Value
Gain	> 36 dB
Bandwidth	> 1 MHz
$V_{O,CM}$	$0.9 \pm 10\%$ V
C_L	1pF

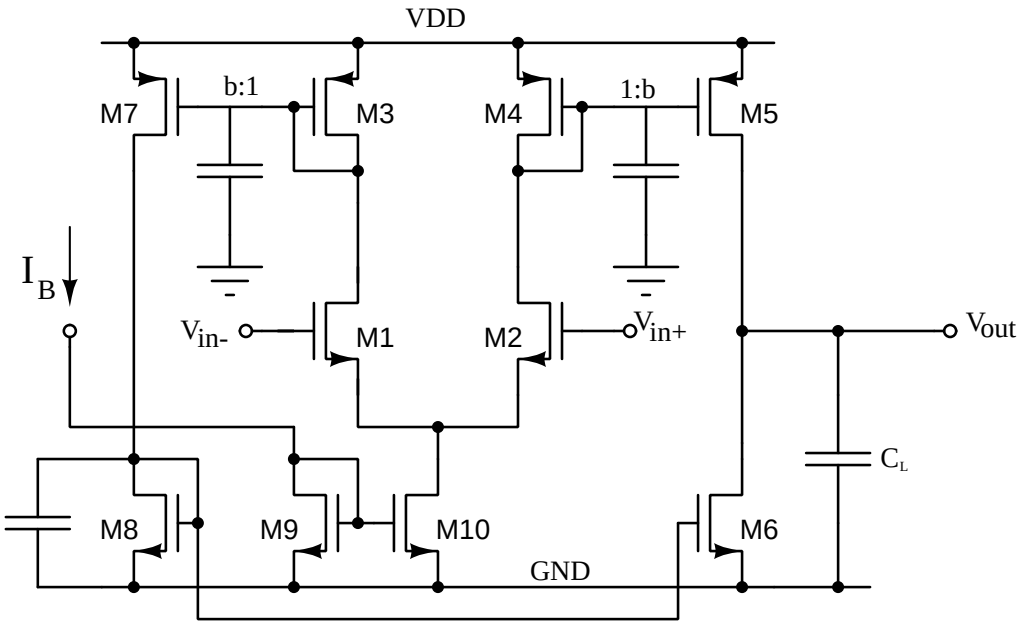

Figure 4: Basic Transconductance Amplifier

- Derive the expression for the DC gain of the circuit as a function of $g_m,\ g_{ds}, C_L, W/L$ ratios of the appropriate transistors [1 Mark(s)]
- Derive the poles and zeros of the circuit without ignoring the parasitic capacitors (club all parasitic capacitors at a node into a single element). Identify the dominant pole and derive the expression for the bandwidth of the circuit [2 Mark(s)]
- Derive the expression for the Slew Rate of the circuit assuming perfect switching and ideal current mirroring when applicable. How would you increase the Slew Rate keeping C_L constant and how would that affect the power consumption? [2 Mark(s)]
  Reference: Design of Analog CMOS Integrated Circuits (2nd Edition) Section 9.9
  Behzad Razavi
- Show the step-by-step design procedure and iterate on the design to meet the specifications in the simulation. Mention the main design iterations and why they didn't work. You are free to use any length (in multiples of $0.18\mu m$) for the nMOSs M6 and M8. Tabulate the final W and L of all the transistors [3 Mark(s)]
- Show the schematic of the circuit with DC Operating points annotated clearly [1 Mark(s)]
- Perform a transient analysis with a 10mV pk-pk sinusoidal input at 10KHz. Plot the input and the output waveforms and clearly mark the peak values. [1 Mark(s)]

- Perform ac analysis and clearly indicate (through markers/cursors) the dc gain and the bandwidth in the bode plot (Must be log-log plot in appropriate units). [1 Mark(s)]
- **Slew Rate:** In this part you need to obtain the slew rate in units of $V/\mu s$ of the circuit. Measure the slope [Hint: Use `deriv` function from the calculator] of the output voltage in the region where it remains fairly constant by switching the differential input voltage from -1.8V to 1.8V with a rise time of 100 ps [Hint: Use `vpwl` from `analogLib` to obtain this input voltage]. Compare this with the analytically calculated Slew Rate. [2 Mark(s)]
- **CMRR:** Using the previously described Common-Mode setup obtain the CMRR of this circuit. Now increase the finger width of M1 by 10% and decrease that of M2 by 10% and re-obtain the CMRR. [2 Mark(s)]
- Tabulate all the parameter values as follows. [1 Mark(s)]

	Hand Calculations	Simulation
Gain Bandwidth Slew Rate DC Power Consumption CMRR		

Part B

Now you'll design a special current mirror circuit. Though you might not see its utility in this part, it might come in handy later. Consider the following circuit. Take M1 and M2 to have equal widths and choose a width such that the node M is close to the $V_{O,CM}$ as in Question 1 Part A.

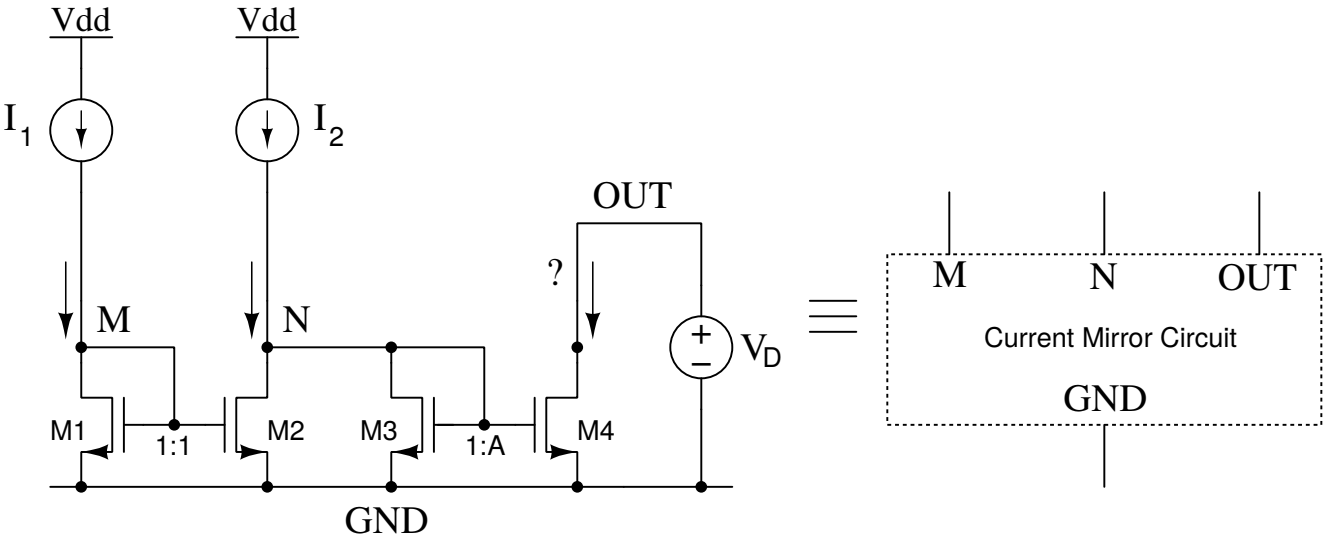

Figure 5: Special Current Mirror Circuit

- Derive the expression for the DC current marked in the circuit schematic for all I_1 and I_2. Assume perfect current mirroring when applicable. [2 Mark(s)]
- Keeping $I_1 = 50\mu A$ and $V_D = 500mV$, sweep I_2 from 60% to 140% of I_1 and plot the output current for the ratio A being 0.5, 1, and 1.5. Explain the deviations of the results from the equation you derived above. [2 Mark(s)]
- Tabulate the region of operation of each MOSFET for three cases when $I_1 >> I_2$, $I_1 = I_2$ and $I_2 >> I_1$ [$>> \implies \sim 10\mu A$ higher] [3 Mark(s)]

Part C

Consider the circuit shown below[2]. Assume M_{11}, M_{12}, M_{13}, M_{14}, M_3, and M_4 have the same W and L and $C_L = 1pF$. Take $A = 0.8$ (of the Current Mirror Block) without violating the finger width criterion mentioned in the general instructions.

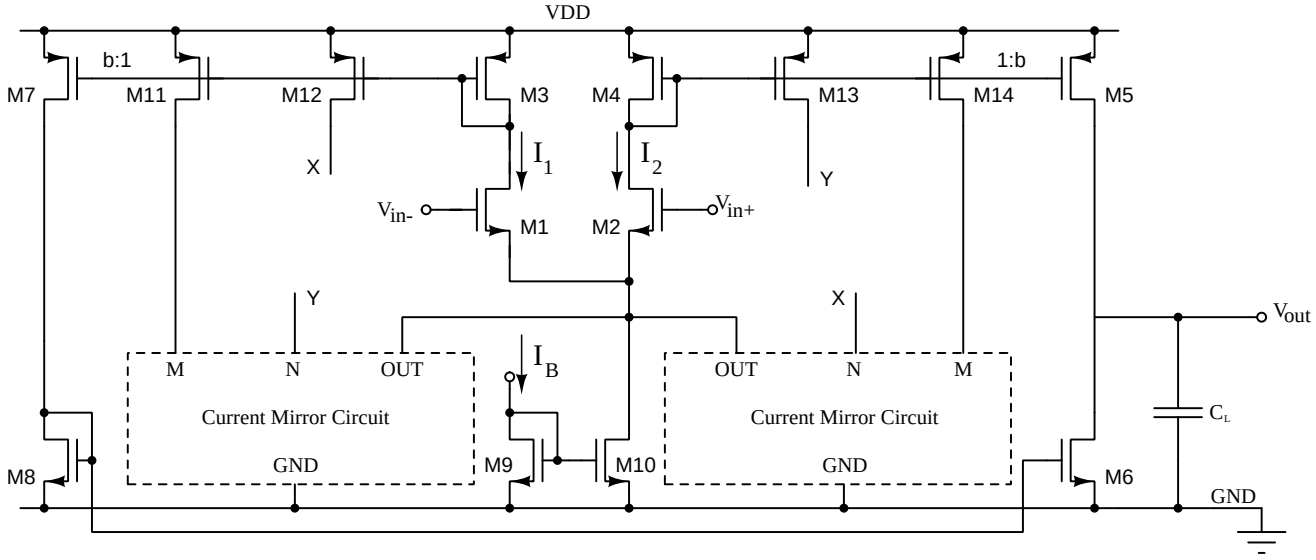

Figure 6: Augmented Differential Amplifier

- Assemble the entire circuit and perform the DC Analysis. Report the schematic with all DC operating point values clearly annotated [2 Mark(s)]
- Derive the expression for the Slew Rate of this circuit in terms of A, assuming perfect current mirroring when applicable and complete switching (Slewing) using two approaches:
  - Assuming instantaneous feedback, obtain the current I_1 and hence the slew rate.
  - Assuming that the feedback from the lower block current-mirrors takes some infinitesimal but finite time, derive the expression for I_1 at every infinitesimal time step and then derive the Slew Rate after infinite such time steps. [Hint: Use the updated Bias Current for the current step as the initial condition for the next step]

  Derive the condition on A for which the feedback becomes unstable. What effect would the instability have in the real circuit? [5 Mark(s)]
- Using the same setup as in Part B obtain the Slew Rate by simulating the circuit with the aforementioned value of A. How does this compare with the Slew Rate in Part A. Has the slew rate improved as expected based on the equation derived above? Why (Describe the non-ideal effects if any)? [1 Mark(s)]
- Now, decrease the tail current to half of your designed value, leaving the rest of the circuit untouched. Perform the Slew Rate analysis again. How does this case compare with the expected improvement? Also compare the power consumption in this case to that if this same Slew Rate were to be obtained using the circuit of Part A.[3] [1 Mark(s)]
- **CMRR:** Using the previously described Common-Mode setup obtain the CMRR of this circuit. Now increase the finger width of M1 by 10% and decrease that of M2 by 10% and re-obtain the CMRR. Compare this with the CMRR in Part A and explain why there is/isn't a difference. [2 Mark(s)]

[2] Well, that escalated quickly. On a serious note, its not complicated if you stare at it for a while

[3] This goes to show that all might seem hunky-dory in theory with ideal assumptions but verification by simulation followed by debugging is necessary

Bonus (Optional)

As a continuation to Question 2, derive the expression for the current I_1 as a function of the input voltage assuming the input MOSFETs are in Weak Inversion/Sub-Threshold Region (for ease of calculation and to obtain a closed-form expression). In this region the I-V relation of the MOSFET is given by

$$I_D = \frac{W}{L} I_0 \exp \frac{V_{GS}}{nV_T}$$

where V_T is the thermal voltage and n is a technology parameter ignoring effect of drain voltage.

- Show that there is a well defined differential input voltage V_{in} for which the current tends to infinity provided the stability condition as derived earlier is violated.
- Show that at large input voltages, this expression reduces to the I_1 expression derived earlier assuming complete switching

For some motivation as to why performing analysis in the Sub-Threshold region is practically applicable and the assumption reasonable, refer to the following papers by Vittoz[1][2] (Optional Reading). [5 Mark(s)]

Enjoy Slewing!

References

[1] J. Fellrath and E. Vittoz, "Small-Signal Model of MOS Transistors in Weak Inversion," *Journées D'Electronique 1977, At Lausanne, Switzerland*, vol. 4, pp. 315–324, Aug. 1977.

[2] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE Journal of Solid-State Circuits*, vol. 12, pp. 224–231, June 1977.