Shashank Obla

sobla@andrew.cmu.edu
+1 412-708-7719

Education

Carnegie Mellon University, Pittsburgh, PA — Aug 2019 – Present
Ph.D in Electrical and Computer Engineering — **3.95/4**
Advised by Prof. James Hoe and affliated with CALCM and the Nexus FPGA Center

Indian Institute of Technology, Bombay, Mumbai, India — Jul 2014 – Jun 2019
B. Tech (Honors) and M. Tech in Electrical Engineering — **9.83/10**
Awarded the **Institute Gold Medal** at the 57th Convocation, IIT Bombay
Specialization in Microelectronics and VLSI with Minor in Biosciences and Bioengineering

Technical Skills

Research Areas
Partial Reconfiguration, Reconfigurable Computing, Computer Architecture, High-Level Synthesis, Memory Systems, High-Performance Computing, Digital Design

Programming
System Verilog, C++, C, VHDL, Bluespec SV, CUDA, OpenMP, OpenCL, MPI, Hadoop

Design Tools
Intel Quartus, Xilinx Vivado Suite, Mentor Modelsim, Cadence - Virtuoso, Genus, Innovus and Voltus, Intel OpenCL SDK for FPGA, VTR Toolchain, Yosys

Research

Dynamic Composability with Partial Reconfiguration (PR) [Presentation]
ECE, Carnegie Mellon University — May 2020 – Present
FPGA design has, since their inception, been limited by the ASIC style of thinking where the design must be provisioned for all usage possibilities during its lifetime. PR allows breaking free from this style of thinking making each design achieve its best for every use case.
To bring this specialization while still retaining the generality of the FPGA fabric is not trivial given architectural limitations and the challenge of developing a generic framework
This project aims to bring Service-Oriented Architecture together with PR to obtain runtime composability of modules while driving architecture design decisions in the Nexus FPGA project

Accelerating Harmonic Balance Analysis for RF Circuits [Dissertation] [Paper]
Electrical Engineering, IIT Bombay — May 2018 – Jul 2019
Master's Thesis; Advisor: Prof. Sachin Patkar
Implementated Harmonic Balance steady-state circuit simulation algorithm for RF circuits and modeled non-linear elements using charge-oriented Modified Nodal Analysis
Optimized LU Decomposition kernel for block-sparse matrices using structure and sparsity aware tuning using the Gilbert-Peierls algorithm

Circuit Partitioning for Distributed Simulation [Dissertation]
Electrical Engineering, IIT Bombay — May 2018 – Jul 2019
Guide: Prof. Sachin Patkar
Worked on digital sequential circuit partitioning for logic simulation over a network of FPGAs
Compared approaches using sub-modular set function based greedy splitting based on Queyranne's algorithm and graph theoretic approaches to minimize communication

Selected Projects

FPGA Tape-Out on TSMC 28nm | *Apple-funded project* — 18-725 & 18-726
Taped-Out a 4x4 FPGA fabric with fast-carry chains and on-chip SRAM
Used VTR along with a self-written bitstream generator to implement the software toolchain
Built test setup using a PYNQ board and a custom PCB for automated test and verification

Selected Projects (contd.)

HBM Abstraction on Stratix 10 MX | *Research Project*

Studied and characterized the HBM channels using various different access patterns
Implemented a CONNECT NoC based switch across the HBM channels to allow for specialized yet abstracted access and analyzed timing to maximize memory bandwidth

D-SOFT Genome Sequence Alignment on FPGA 18-643

Studied and implemented the D-SOFT algorithm (from the Darwin coprocessor)
Compared the performance and area of an HLS-only implementation vs implementations using different NoCs to extract data-dependent parallelism

Pipelined RISC Processor

Designed and Implemented a 16-Bit, 6-Stage Pipelined RISC processor based on a Turing-Complete ISA in VHDL and successfully tested the implementation on a Cyclone IV E FPGA along with a self-designed UART based DMA bootloader
Included branch predictor, data and control and hazard mitigation unit to improve performance

Simple High-Level Synthesis Tool

Implemented the HLS flow, generating synthesisable VHDL code, of Scheduling, and Binding for arithmetic expressions and optimized hardware synthesis with shared variable identification under resource and timing constraints input on a GUI

Teaching

Graduate Teaching Assistant
18-643 Reconfigurable Logic; Prof. James Hoe — Fall 2020

Graduate Teaching Assistant
EE619 RF IC Design; Prof. Rajesh Zele — Spring 2019
Received a certificate for *Excellence in Teaching Assistantship*

Graduate Teaching Assistant
EE618 CMOS Analog IC Design; Prof. Rajesh Zele — Fall 2018
Received a certificate for *Excellence in Teaching Assistantship*

Other Activities

Junior Design Engineer
IIT Bombay Racing, IIT Bombay — Aug 2015 – Jul 2016

Part of IIT Bombay Racing Team of 70 students to design and fabricate India's **Fastest Electric** Racecar for **Formula Student UK**, an International Racecar Competition
Implemented the CAN protocol, designed onboard data acquisition and live wireless telemetry

National Social Service, India
Computer Literacy Programme and Lend Your Voice — Jul 2014 – Jul 2016

Volunteered in the NSS Summer Volunteering Program to teach basic computers
Recorded magazines for the LYV initiative to create audiobooks for the visually challenged

Relevant Courses

Computer Architecture and Digital VLSI
Reconfigurable Logic, Advanced Digital IC Design, VLSI Design, Systems Design, Testing and Verification of VLSI Circuits, Foundations of VLSI CAD, VLSI Design Lab, Processor Design

Computer Systems
Intro to ML (PhD), Compiler Design, Data Structures and Algorithms, Operating Systems

Analog VLSI
CMOS Analog VLSI Design, Mixed-Signal VLSI Design, RF Chip Design, Analog Circuits