

Development of High Impedance Measurement System for Water Leakage Detection in Implantable Neuroprosthetic Devices *

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Abstract— There has been a push for a greater number of channels in implantable neuroprosthetic devices; but, that number has largely been limited by current hermetic packaging technology. Microfabricated packaging is becoming reality, but a standard testing system is needed to prepare these devices for clinical trials. Impedance measurements of electrodes built into the packaging layers may give an early warning of device failure and predict device lifetime. Because the impedance magnitudes of such devices can be on the order of gigaohms, a versatile system was designed to accommodate ultra-high impedances and allow future integrated circuit implementation in current neural prosthetic technologies. Here we present the circuitry, control software, and preliminary testing results of our designed system.

I. INTRODUCTION

Implantable medical devices use hermetic packaging to protect electronics inside the body. Modern implantable neural interface devices, such as retinal prostheses [1] or motor neuroprostheses [2], require hundreds of channels and may grow to over 1000 channels in the future, beyond the capacity of typical titanium or ceramic packages. Microfabricated packages are under development [3], but lack an accepted method for hermetic testing for clinical use. Traditional titanium or ceramic packages use helium leakage to test hermeticity; but, microfabricated packages lack empty internal space. We propose adding inter-digitated electrodes between layers of a microfabricated package and continually measuring the impedance to project device lifetime. Here we present an impedance-sensing method as an early leakage warning system for implantable microfabricated medical devices [4].

The development of reliable and portable impedance measurements systems has become a central focus on biomedical research and applications. For such research, implanted electrodes may perform well in the short term but fail over longer periods of time. Several impedance measurement systems have been designed for many uses. For example, uses include the monitoring of tissue electrode interactions in bladder stimulations as well as ischemia monitoring [5],[6],[7]. However, systems presented in [5]

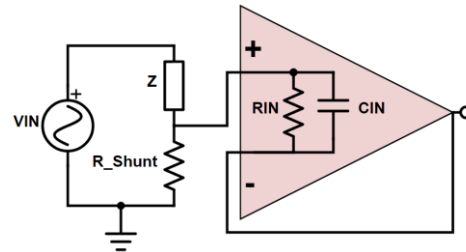


Figure 1. Schematic concept of impedance measurement system. Current through the unknown impedance passes through a known resistance, and that voltage is amplified and digitized.

and [6] only operate in the range of a few ohms to several kilohms. If the electrode impedances are much larger than this range, which oftentimes are, then the system will not be adequate. Other systems rely on complicated lock-in amplifiers that would decrease the feasibility for an integrated circuit approach due to power consumption and economic considerations [8]. For the purposes of this study, a portable and cost-effective impedance measurement system was designed to allow for the measurements of impedances from 100 Ω -10 G Ω for future integration in a recently developed neural prosthetic, which currently lacks water leakage detection [9]. Because of this system can be designed from discrete electrical components, its applications transcend beyond water leakage detection. It can be used for general impedance measurements in cost-effective research settings, since the discrete components can be purchased for less than \$20, while commercial automated impedance measurements cost dozens of thousands of dollars.

It is important to note that since the chief feature of this system is to detect impedance changes over large ranges, this paper simplifies the circuit analysis techniques of the system. In practice, first order approximations are overly simplified, since there are multiple implicit capacitances (Fig.1) that should be analyzed for ultra-high accuracy systems [10]. However, for the purposes of the system's applications, these non-idealities can be ignored.

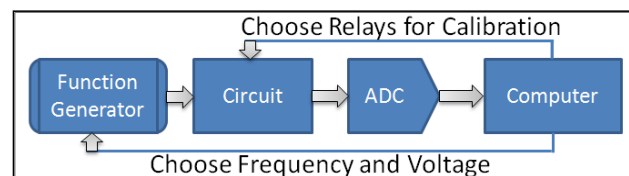


Figure 2. Block Diagram of Impedance Measurement System.

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II. SYSTEM OVERVIEW

A visual overview of the impedance measurement system is shown in Fig. 2. A computer running LabVIEW controls a function generator that produces the input voltage to the current sense circuit; this input voltage is denoted as $V_{in}(t)$. The computer also calibrates the current sense circuit by choosing appropriate gain and shunt resistors. The outputs of the ADC are directed to the computer, which performs Fourier Analysis to obtain the unknown impedance.

III. CIRCUIT DESIGN AND IMPLEMENTATION

In order to measure the unknown impedance, a known voltage source was connected to a designed current sense circuit; its simplified version is shown in Fig. 3, while the detailed version useful for recreating the system is shown in Fig. 4. The first portion of the circuit in Fig. 3 includes a voltage divider of the unknown impedance in series with a known shunt resistor. To sense the current that traverses through both the shunt resistor and the unknown impedance, an operational amplifier buffer is utilized to prevent loading between the amplifying stage (right-most amplifier) and the shunt resistor. From impedance voltage division, the input of the leftmost amplifier is given by

$$V_1(j\omega) = \frac{V_{in}(j\omega) \times R_{Shunt}}{R_{Shunt} + Z}, \quad (1)$$

where $V_1(j\omega)$ and $V_{in}(j\omega)$ are the frequency-dependant phasor representations of $V_1(t)$ and $V_{in}(t)$, respectively. $V_1(t)$ and $V_{in}(t)$, shown in Fig. 3, are time-dependent voltages. $V_1(t)$ corresponds to leftmost non-inverting operational amplifier input, while $V_{in}(t)$ corresponds to the voltage of the function generator. Furthermore, R_{Shunt} is one of the 4 bottom-left shunt resistors of Fig. 3 chosen by an electromagnetic relay, and Z is the complex-valued unknown impedance. As the impedance magnitude increases, the amplitude of $V_1(t)$ decreases and becomes more susceptible to noise. Therefore, amplification from second operational amplifier is necessary. Assuming an ideal operational amplifier model, the gain of the second amplifier is

$$gain = \frac{V_{out}(j\omega)}{V_1(j\omega)} = -\frac{R_{Gain}}{1k\Omega}, \quad (2)$$

where R_{Gain} is 1 k Ω , 10 k Ω or 100 k Ω . Substituting (1) into (2) yields the transfer function of the system:

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{R_{Shunt} \times gain}{R_{Shunt} + Z}. \quad (3)$$

As previously stated, ideal operational amplifier models were assumed. This approximation holds at sufficiently low input frequencies. However, the approximation breaks at high input frequencies (above 100 Hz for a gigaohm impedance). The reason stems from the interactions between the input capacitance of the amplifier and the equivalent

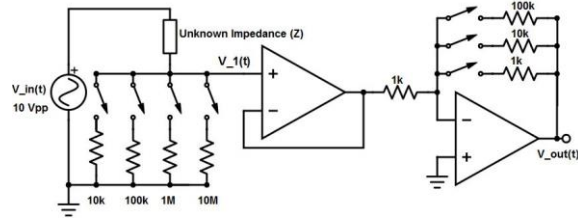


Figure 3. Implementation of a wide-range impedance spectroscopy system.

resistances from the perspective of its input terminals. In general, the implicit low pass filter constructed from parallel resistance and the input capacitance can generate phase and magnitude calculation errors, as shown in Fig. 1. Therefore, the method presented in this paper works best with low input frequencies.

The non-zero bias current of an operational amplifier can cause an unintended DC offset at the output, and thus, fosters impedance calculation errors. To circumvent this issue, pico-ampere bias current operational amplifiers as well as software corrective actions were utilized. Also, the techniques of adequate grounded shielding, soldering rather than bread boarding, and minimizing wire length were used during circuit development to abate interference and noise. Since the circuit was designed with discretely soldered components, an integrated circuit implementation of this system would curb the parasitic capacitance by at least an order of magnitude and further increase the range capabilities of this system.

IV. SOFTWARE DESIGN AND IMPLEMENTATION

The software of the system, which generates a Bode Plot of the unknown impedance, was written in National Instruments LabVIEW 2011. This graphics-based programming language allows I/O among the computer running the application, an Agilent 33220A voltage function generator, and a National Instruments PCI-6111 board that supports Analog to Digital Conversion (ADC) and writing to digital ports.

To summarize the overall code structure, the program is fundamentally composed of triple-nested while loops in the following order from innermost to outermost: gain resistor choice, shunt resistor choice, and function generator frequency choice. For a specific frequency, the function generator is set to 10 V_{pp}. Then, the shunt and gain resistor are both set to the maximum setting: 10 M Ω and 100 k Ω , respectively. To prevent operational amplifier saturation, the output voltage is sampled and if the absolute value of the peak or trough of the output voltage is more than 2.2 V (assuming the positive and negative supplies of the rail-to-rail operational amplifiers are ± 2.5 V), the gain resistor is repeatedly decreased until the saturation ends. If this clipping does not terminate when the chosen gain resistor is set to the smallest possible value, the shunt resistor is stepped down by a factor of 10 and the maximum gain resistor is reinstated (100 k Ω). Then, in an identical fashion as described previously, the gain resistor is adjusted, if necessary. If both shunt and gain resistors are minimized, the

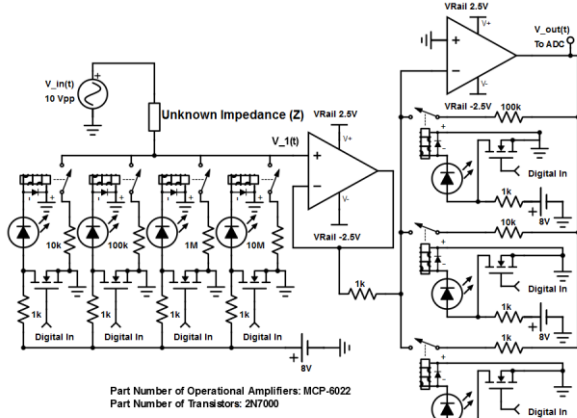


Figure 4. Detailed implementation of the impedance spectroscopy system. Digitally-controlled relays switch in different resistor values based on the amplitude of the measured signal, until the signal is in the middle of the range of the analog to digital converter.

function generator voltage is repeatedly divided by a factor of two until the output voltage is in the desired range.

To minimize noise error, we ensured that the output voltage amplitude is at least the designated noise threshold of 0.2 V. However, this condition is always satisfied because of the order by which the shunt and gain resistors are chosen.

For ADCs, errors from frequency aliasing, quantization noise, and white noise must be avoided. To prevent aliasing, the Nyquist Sampling Theorem was invoked, which states that the sampling rate must be greater than twice the largest frequency of the band-limited signal [11]. For example, for a 10 Hz input sinusoid, oversampling the signal at a rate of 1 kHz can prevent these errors; but, the sampling rate will need to be increased accordingly for larger input frequencies. Besides sampling rate, a second parameter of ADCs is a choice of the number of samples. For our system, we found that collecting data for three time periods of the specific frequency achieves a reasonable balance between accuracy and time-optimization. A reasonable sampling duration, therefore, is $3/f$, where f is the frequency of the input voltage. The sampling period is simply the reciprocal of the sampling frequency (Sf), which we will consider to be 1 kHz. Thus, an adequate number of samples is

$$\frac{3 \text{ time periods}}{\text{sampling period}} = \frac{3 \times Sf}{f} = \frac{3000}{f}. \quad (4)$$

To complete the impedance calculation, suppose we rearrange (3) from the *Circuit Design & Implementation* section:

$$\frac{1}{\text{gain}} \times \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{R_{Shunt}}{R_{Shunt} + Z}. \quad (5)$$

The left-hand side of (5) can be found by writing it in polar form and since it is a complex number, there exists real numbers A and θ such that

$$Ae^{j\theta} = \frac{1}{\text{gain}} \times \frac{V_{out}(j\omega)}{V_{in}(j\omega)}. \quad (6)$$

To correctly determine the magnitude A of this complex number, the amplitudes of the input and output sinusoidal voltages must be determined. For consistency, we will adopt the notation used in signal processing texts. For example, because the $V_{out}(t)$ and $V_{in}(t)$ channels were sampled and converted to discrete-time signals, this paper will henceforth associate the discrete-time signals with brackets to differentiate them from continuous-time signals. So, the discrete (and zero average-valued) counterparts of the continuous signals $V_{in}(t)$ and $V_{out}(t)$ will be referred to as $V_{in}[n]$ and $V_{out}[n]$, respectively. Note that as a consequence of the operational amplifier bias current, the $V_{out}(t)$ may contain an undesired DC offset. The error of this offset can be removed by a software-based correction that element-wise subtracts the DC offset from the output; the result of this operation is $V_{out}[n]$. Making these modifications leads to the following equation:

$$A = \left| \frac{V_{OUT}}{\text{gain} \times V_{IN}} \right|, \quad (7)$$

where V_{IN} and V_{OUT} are corresponding amplitudes of the sampled discrete sequences $V_{in}[n]$ and $V_{out}[n]$.

To facilitate the calculations of θ , Fourier analysis techniques were employed. Because a properly biased operational amplifier circuit can be modeled as a Linear and Time-Invariant System (LTI), the output frequency of the circuit is the same as the input frequency. Therefore, the output, $V_{out}[n]$, will be a scaled and time-shifted version of the input $V_{in}[n]$. According to the time-shift property of the discrete time Fourier transform, a shift in time corresponds to multiplication by a complex exponential in the frequency domain [11]. Therefore, if the complex exponential can be derived, the phase of the impedance can be determined. By using the principle value of the complex natural logarithm, the phase of a discrete-time sinusoidal function $x[n]$ with respect to a cosine of identical frequency and zero phase shift can be mathematically represented as:

$$\text{phase}\{x[n]\} = -j \times \ln \left\{ \tan^{-1} \left[\frac{\text{Im}\{\mathcal{F}\{x[n]\}_{Har}\}}{\text{Re}\{\mathcal{F}\{x[n]\}_{Har}\}} \right] \right\}. \quad (8)$$

For the above expression, $j = \sqrt{-1}$. Furthermore, $\mathcal{F}\{x[n]\}_{Har}$ represents the value of the Fast Fourier Transform at the negative harmonic of the sampled discrete-time sinusoid $x[n]$. Additionally, Im and Re respectively calculate the imaginary and real parts of a complex number. Note that caution must be exercised when computing the arctangent of (8). When measuring highly capacitive impedances, it is possible that computation may yield a slightly negative $\text{Re}\{\mathcal{F}\{x[n]\}_{Har}$, when ideally it would be zero. As a result, an erroneous phase of $\pi/2$ may be obtained instead of the correct phase of $-\pi/2$. Next, in order to find the phase between the sampled output and input voltage sequences $V_{out}[n]$ and $V_{in}[n]$, respectively, θ is calculated. Therefore,

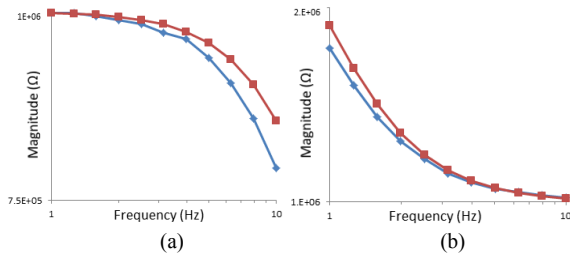


Figure 5. Magnitude measurement data from (a) a parallel resistor-capacitor and (b) a resistor in series with a parallel resistor-capacitor. Red (large squares) shows theoretical data while blue (small squares) shows measured data.

$$\theta = \text{phase}\{V_{out}[n]\} - \text{phase}\{V_{in}[n]\} + \pi. \quad (9)$$

Note that θ is not the phase of the impedance, but rather an intermediate step in the calculation. Also, instead of scaling the $V_{out}[n]$ sequence by the negative gain factor, π is introduced into the previous equation for computational efficiency. Combining (6), (7), (8), and (9) and rearranging yields the sought complex-valued unknown impedance Z :

$$Z = \frac{R_{shunt}}{Ae^{j\theta}} - R_{shunt} \quad (10)$$

V. TESTING RESULTS

To corroborate that the system functions adequately, it was tested against several known impedances composed of a variety of different passive elements. A 1 G Ω resistor, 5 G Ω resistor, and 50.72 pF capacitor were measured with the system at frequencies ranging from 1 Hz to 10 Hz. The resistor measurements showed accuracy over 97% in magnitude and phase, while the capacitor measurement showed accuracy of 96%. Next, measurements were made on a parallel combination of a 1 M Ω resistor and a 10 nF capacitor, followed by measurements on a 1 M Ω resistor in series with a parallel combination of a 1 G Ω resistor and a 0.1 μ F capacitor. These results are shown in Figs. 5 (magnitude) and 6 (phase). Figs. 5a and 6a convey the 90-95% accuracy rating of this test. However, in some cases the lower accuracy of certain tests involving capacitors may stem from precision of the components used. The last test, shown in Figs. 5b and 6b, yielded an accuracy of 98%.

VI. CONCLUSION

In order to measure the water leakage of implantable neuroprostheses in the human body, a versatile automated ultra-high impedance measurement system was developed. The hardware component of the system is a current-sensing circuit that is calibrated appropriately based on the practical choosing of a shunt resistor and gain resistor. The software portion performs the calibration of the hardware by specifying a pragmatic choice of gain and shunt resistors. Preliminary testing of the system has proven successful; the system accurately measures the magnitude and phase of large impedances at low frequencies. Future work in improving the frequency range of the system may include using more accurate circuit models to accommodate the

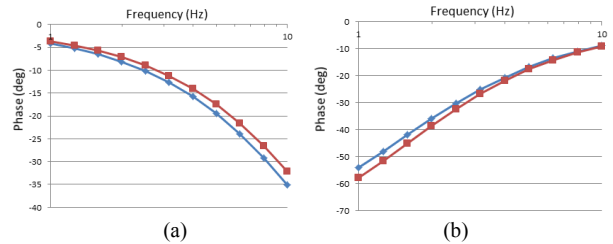


Figure 6. Phase measurement data from (a) a parallel resistor-capacitor and (b) a resistor in series with a parallel resistor-capacitor. Red (large squares) shows theoretical data while blue (small squares) shows measured data.

phase and magnitude calculation errors stemming from devices parasitics.

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