2.5 Minimally Invasive Retinal Prosthesis

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Over 14 million people worldwide suffer from blindness due to age related macular degeneration and retinitis pigmentosa. Blindness results from loss of photoreceptors, but other retinal neurons maintain an active connection to the brain. We are developing a chronic retinal implant in hopes of restoring vision to these patients. The goal is to stimulate the remaining healthy layers of retinal neurons using brief biphasic current pulses. Design requirements include: 1) an external source (i.e. no batteries), 2) wireless communication of external commands to the implant and 3) wireless tuning of pulse amplitude, duration and interpulse timing. The first and second were met by an inductively coupled power and data link. The third was enabled by a flexible stimulator chip architecture that allows for seamless scaling of the number of electrodes that can be driven. Physical implant design is based on a minimally invasive approach, shown schematically in Fig. 2.5.1. Only the electrode array is placed in the eye (beneath the retina), while the secondary coils and stimulator chip are surgically attached to the eyeball. Surgical trauma to the eye is greatly minimized by placing the bulky electronics in the more compliant eye socket rather than the delicate retina. Heat generated by the chip is also safely dissipated there. This approach lets the implant be safely removed after surgery if necessary. The implant (see mockup in Fig. 2.5.1) is made from a paralyene-encapsulated flexible polyimide substrate onto which the chip and electrode array are stud bump bonded.

The stimulator chip architecture in Fig. 2.5.2 provides frequency-independent operation and compensates for non-idealities due to process, temperature and voltage. Power from an inductive link is rectified and filtered using off-chip diodes and capacitors housed on the flexible substrate, with the ±2.5V supply voltage regulated by an off-chip Zener. Amplitude shift-keyed modulated digital data are received through a separate secondary, concentric to the power coil. Nominal carrier frequencies for power and data are 125kHz and 13.56MHz respectively. The front-end decouples the power and data signals and demodulates and restores the data signal to digital levels. The symbol is encoded as a pulse-width modulated signal [4], a 50-50% duty cycle encoding a 0 and 30-70% duty cycle encoding a 1. Data rate can be varied from 50kb/s to 700kb/s. Data and clock are recovered by a delay-locked loop (DLL) and fed to a control logic block. Control block signals direct the current driver array, which outputs biphasic current pulses to the electrode array. The chip can drive a total of 15 electrodes, contains 30,000 transistors in a 0.5μm technology (3M2P), occupies an area of 2.3×2.3mm² and consumes 1.3mW at a data rate of 100kb/s, excluding the current sources.

A transistor-based envelope detector in Fig. 2.5.3 demodulates the data. It exploits the fact that source coupling of NMOS transistors leads to the source following the greater of the input signals [1, 2]. To restore the small signal output of the envelope detector while maintaining pulse width integrity, a single-to-differential converter based on peak locking was designed and is shown in Fig. 2.5.3. In the peak-locked loop, the incoming signal is inverted with unity gain with an arbitrary reference level using a differential-difference amplifier (DDA) [3], the peak of this

waveform is compared with a buffered (using another DDA) version of the incoming signal and the difference drives a charge pump which moves the reference level. This locks the two signals and creates a truly differential signal which is fed to a comparator. Clock and data recovery is performed by a DLL similar in architecture to [4] but not in circuit detail. The adaptive bandwidth DLL was designed using a low power and area technique [5] shown in Fig 2.5.4. The nand-based phase-only detector provides robust operation under noisy clock conditions and prevents the DLL from getting pegged at one end of its tuning range. The regulator features constant damping adaptive compensation (based on a variant of the idea in [6]) and dynamically provides the load current which reduces power. The chip can receive four 16 bit commands: Configure, Pulse-Up, Pulse-Down and Stop. Each command is decoded by a state machine which provides the appropriate signals to the current driver in Fig. 2.5.5. The Configure command tells the chip that the next 170 bits are part of the data sequence. To provide a large range of timing options and clock-frequency-independent operation, the duration of the Pulse-Up and Pulse-Down commands is the difference between the arrival times of the Pulse-Up or Pulse-Down commands and the Stop command. The current sources have a range of 0-930μA in steps of 30μA. The adjustable electrode bias in Fig. 2.5.5 increases the maximum charge capacity of the electrode.

Results in Fig. 2.5.6 from a board prototype were obtained with the chip powered through an inductive link driven by a class E power amplifier operating at 125kHz. Data was provided via another inductive link driven by a class A power amplifier operating at 8.2MHz due to receiver coil limitations. The primary and secondary of both links were separated by 15mm. The class A amp was driven by a LabView PXI system controlled through a custom designed software interface. The following commands were issued in sequence periodically: Configure followed by 170 bits of data, Pulse-Down followed by Pulse-Up after 1ms. A current output of 90μA was fed to a 400μm diameter iridium oxide electrode in saline and the voltage across the electrode is shown.

References:
[1] C. A. Mead, "Analog VLSI and Neural Systems," 1st Ed. Addison Wellesley Publishing Company, 1989
[2] I.E. Opris, "Rail-to-Rail Multiple-Input Min/Max Circuit", IEEE Trans. CAS II, vol. 45 , no. 1, pp. 137 –140, Jan., 1998.
[3] E. Sackinger and W. Guggenbuhl, "A Versatile Building Block: the CMOS Differential Difference Amplifier", IEEE J. Solid-State Circuits, vol. 22, no. 2, pp. 287 – 294, Apr., 1987
[4] W. Liu el al., "Neuro-Stimulus Chip with Telemetry Unit for Retinal Prosthetic Device," IEEE J. Solid-State Circuits, vol. 35, no. 10, pp. 1487 – 1497, Oct., 2000.
[5] M. Lee, W. Dally and P. Chiang, "Low Power Area-Efficient High Speed I/O Circuit Techniques," IEEE J. Solid State Circuits, vol. 35, no. 11, pp. 1591-1599, Nov., 2000.
[6] J G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE J. of Solid State Circuits, vol. 31, no. 11, pp. 1723-1732, Nov., 1996.
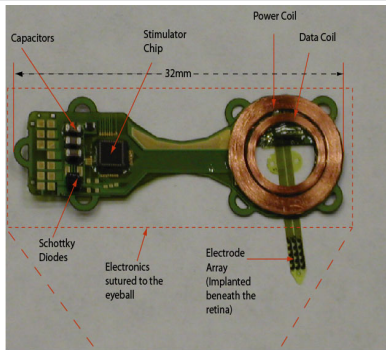
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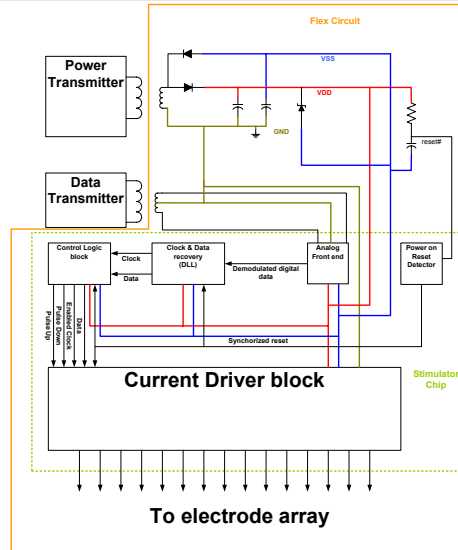Figure 2.5.1: Schematic of the minimally invasive prosthesis.

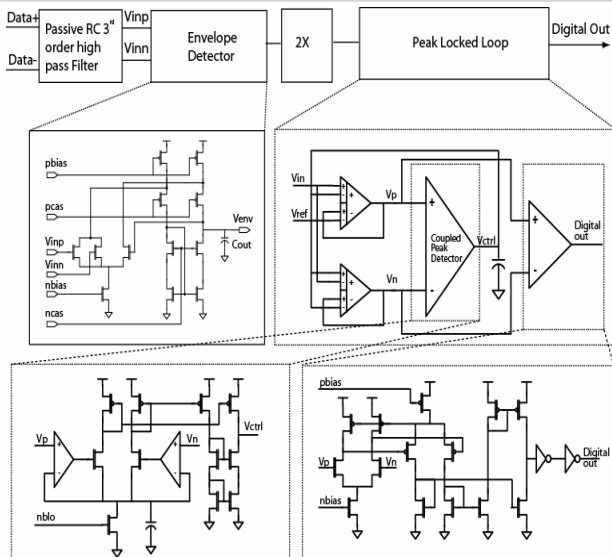Figure 2.5.2: Architectural overview of the implant.

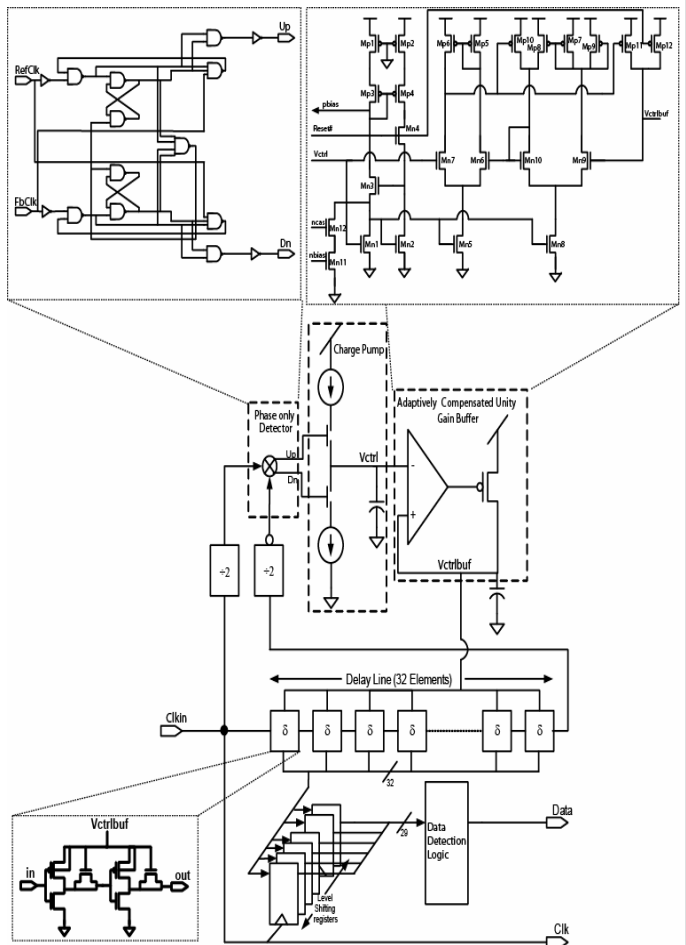
Figure 2.5.3: Schematic of the analog front-end.

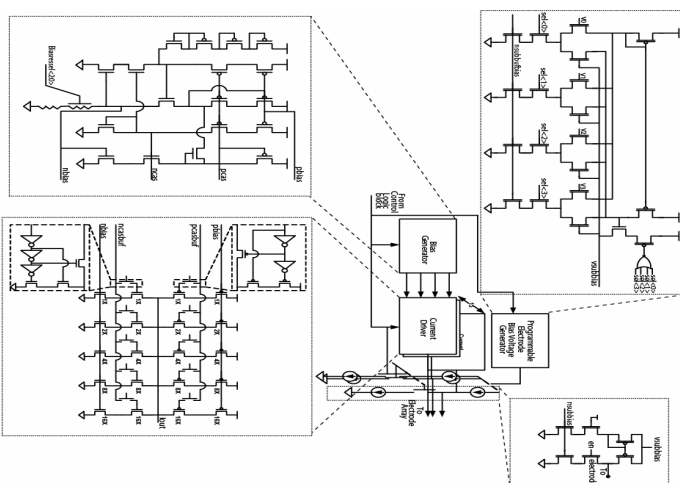Figure 2.5.4: Low Power Clock and Data recovery block.

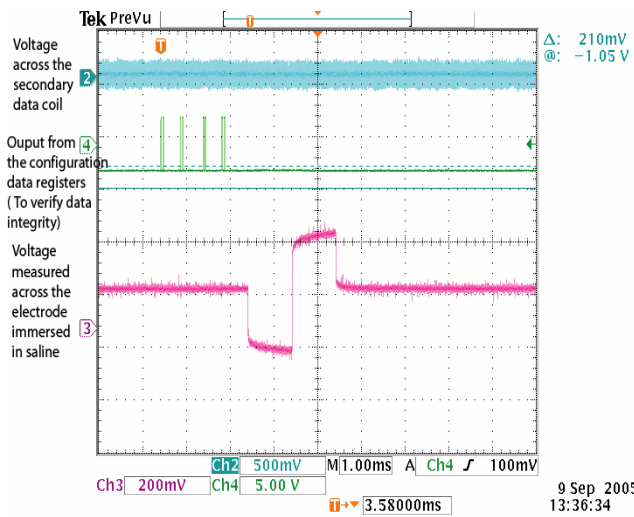Figure 2.5.5: Programmable Current Driver with adjustable electrode bias.

Figure 2.5.6: Output of the wirelessly driven and powered stimulator chip driving an electrode immersed in saline.
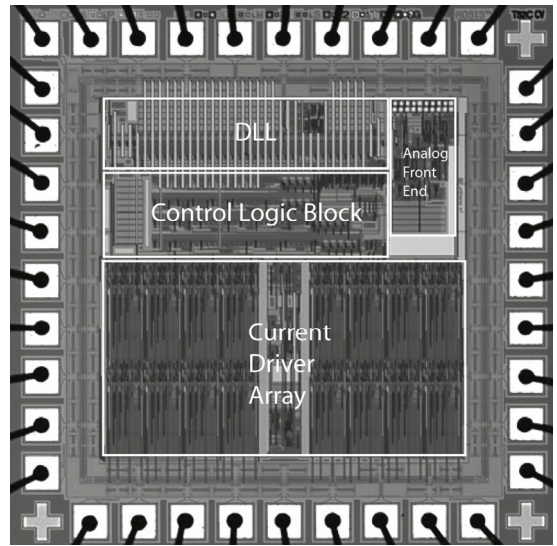

Figure 2.5.7: Micrograph of the implantable stimulator chip.