Silicon Nano-transistors and Silicon Nanotechnology for High-Performance Logic Applications

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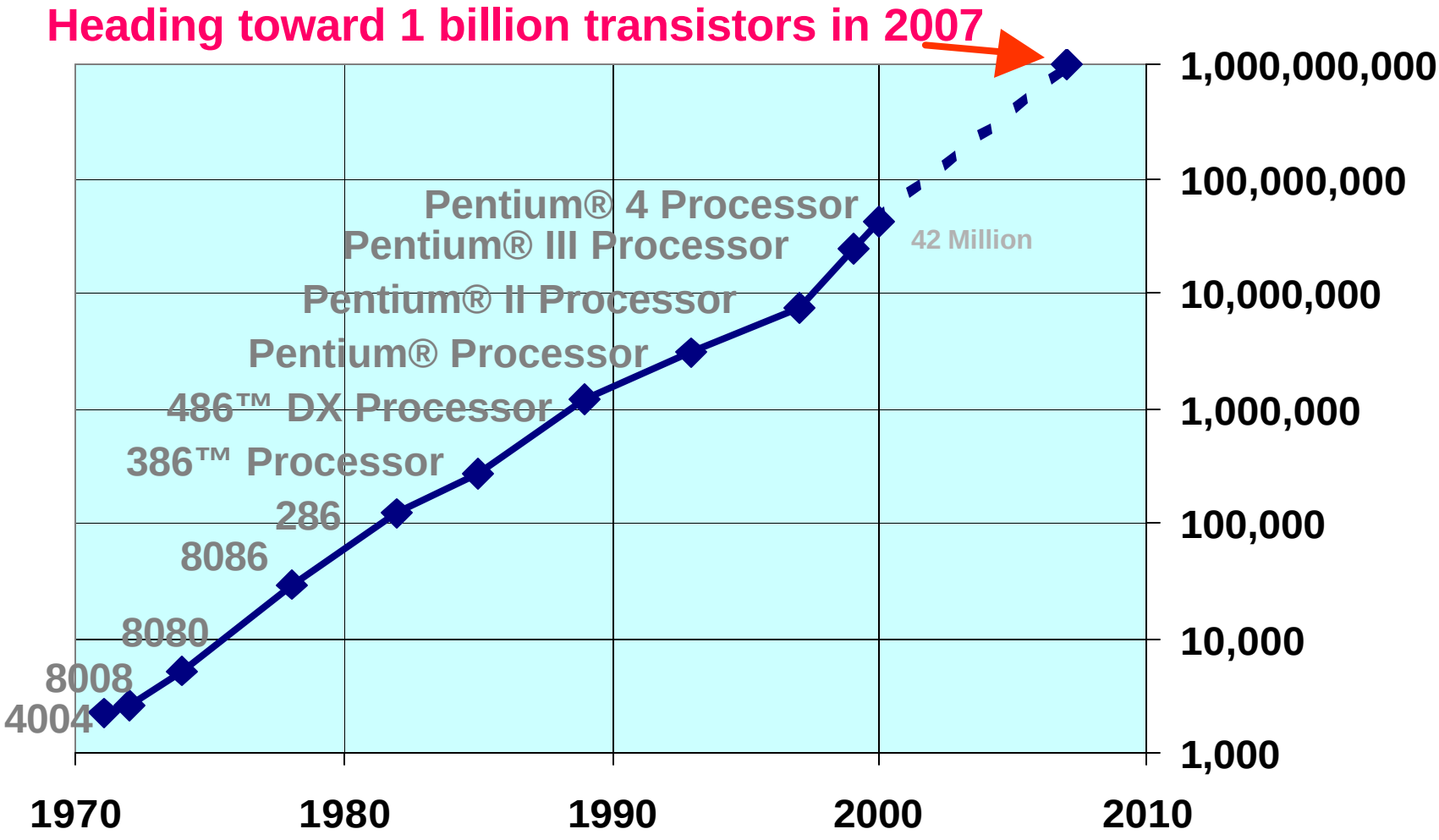
Content

- **Transistor scaling and Moore's law**
- **Silicon nano-transistors and new device architecture**
- **Examples of Silicon nano-technology**
- **Theoretical scaling limit for Si device**
- **Summary**

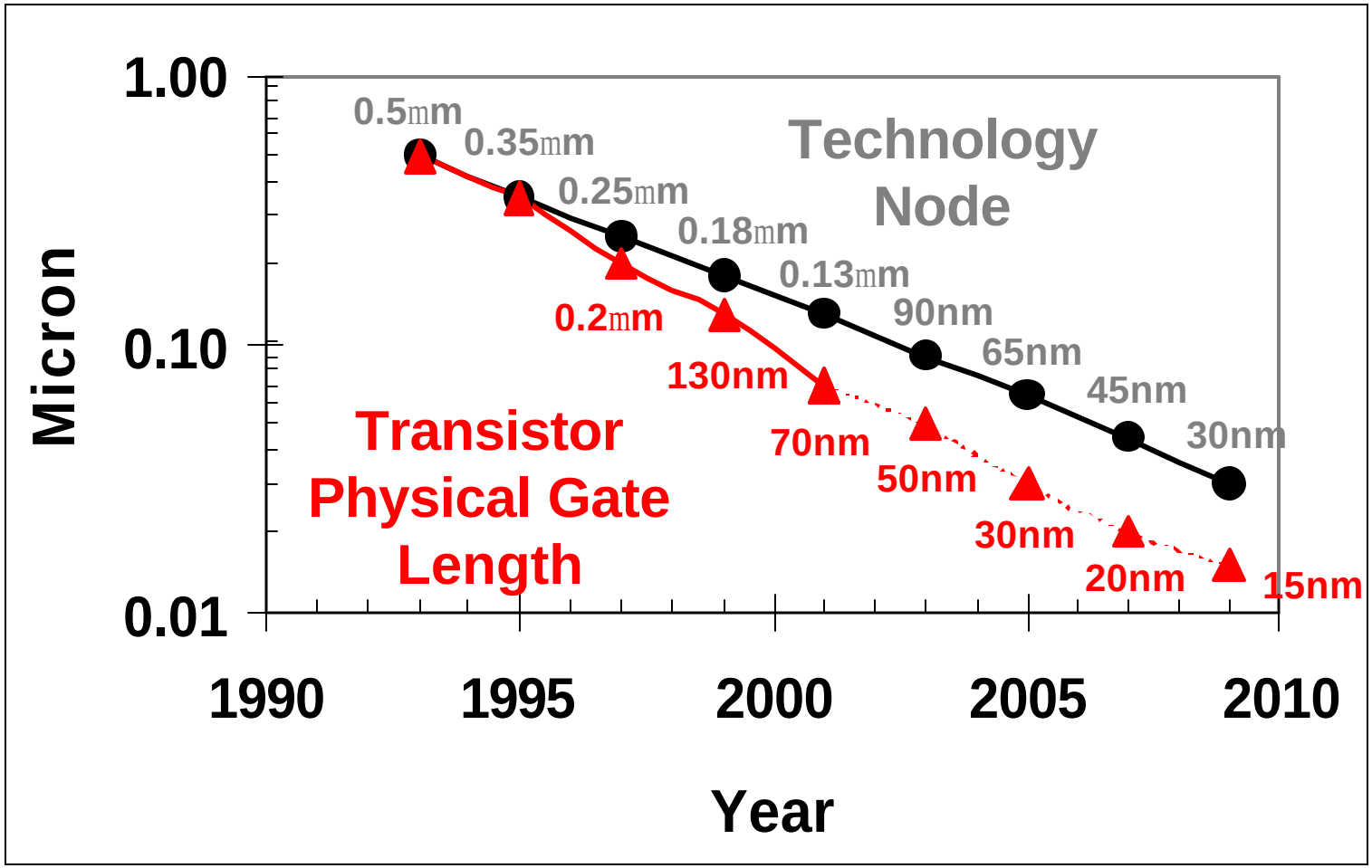
Moore's Law Continues…

– Transistor # doubling every 2 years toward the 1 billion transistor microprocessor



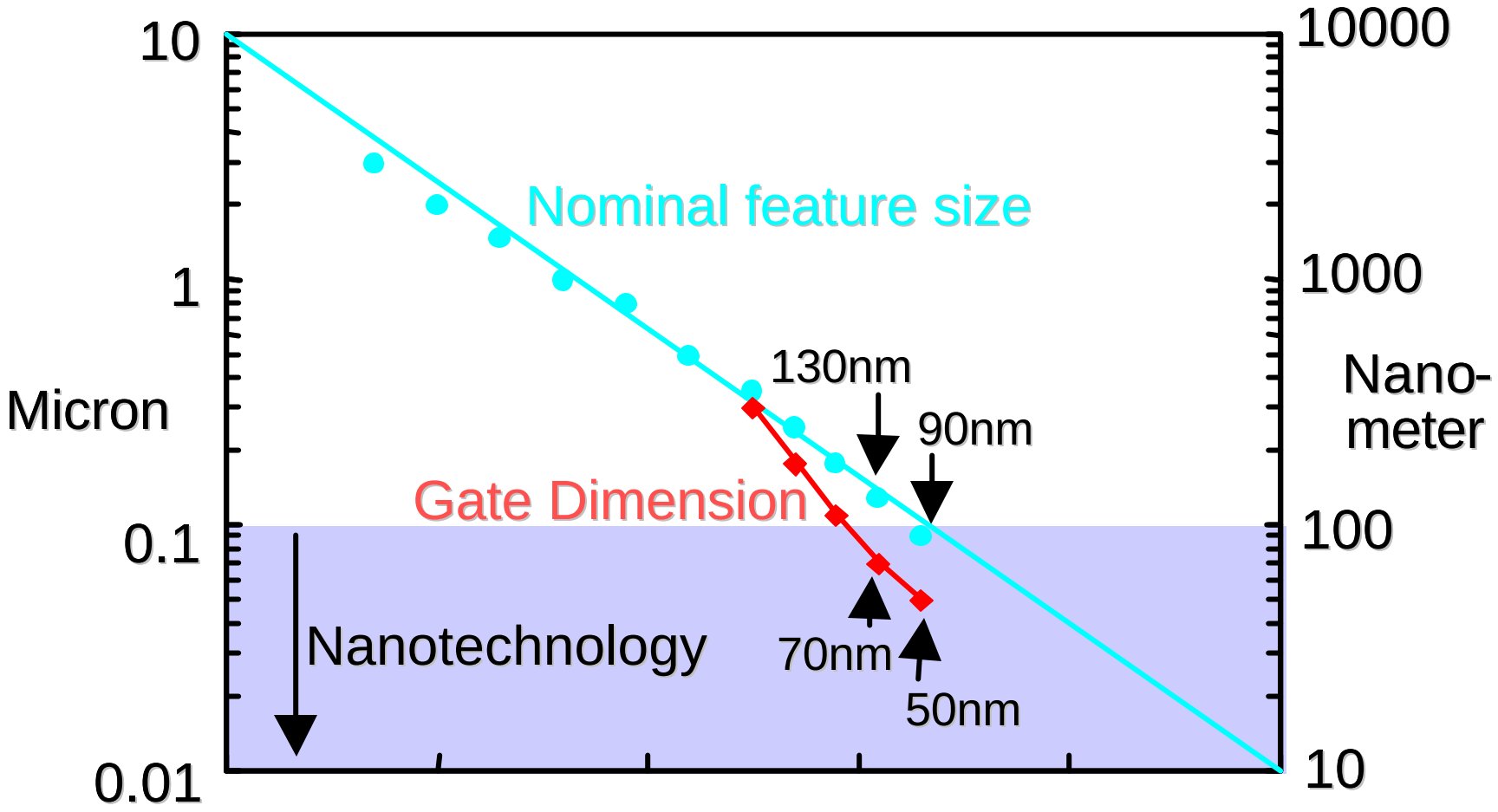
>220M transistors integrated into devices produced today

Transistor Physical Gate Length Requirement

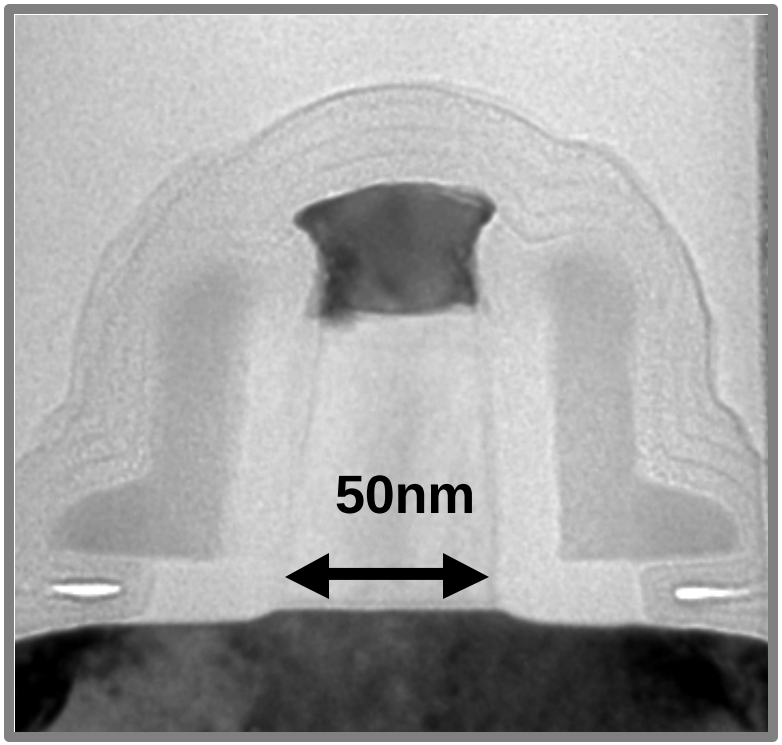


Transistor physical gate length will reach ~15nm before end of this decade, and ~10nm early next decade

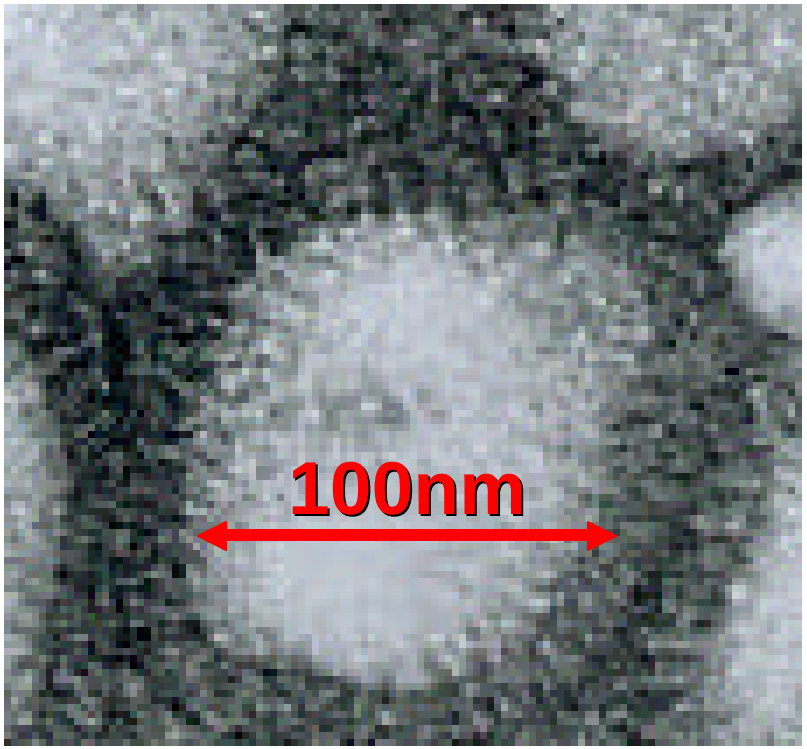
Silicon Nanotechnology has already been in production



Production Transistors Smaller Than Virus



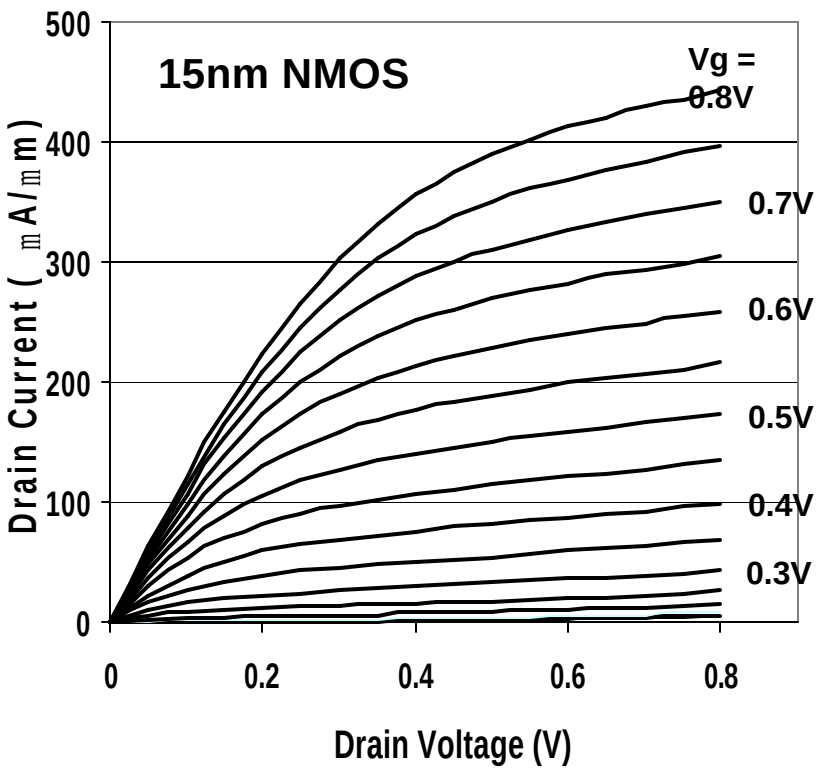
Si transistor in the 90nm logic technology node: currently in production

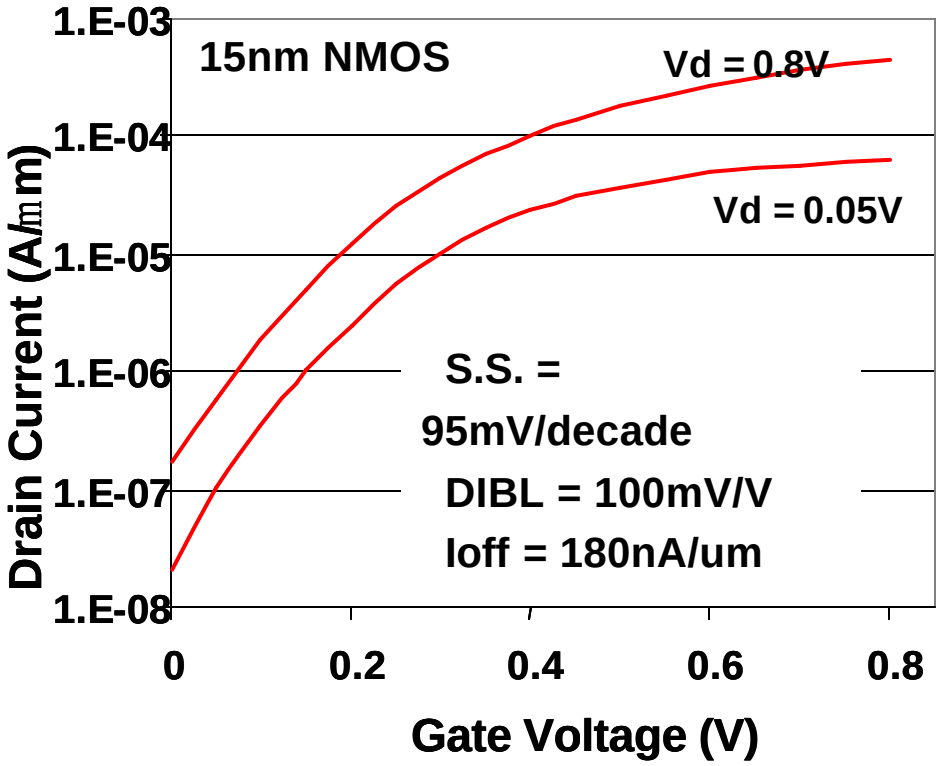


Influenza virus

Source: CDC

Experimental 15nm Si Transistor





- **Well-controlled short channel characteristics**

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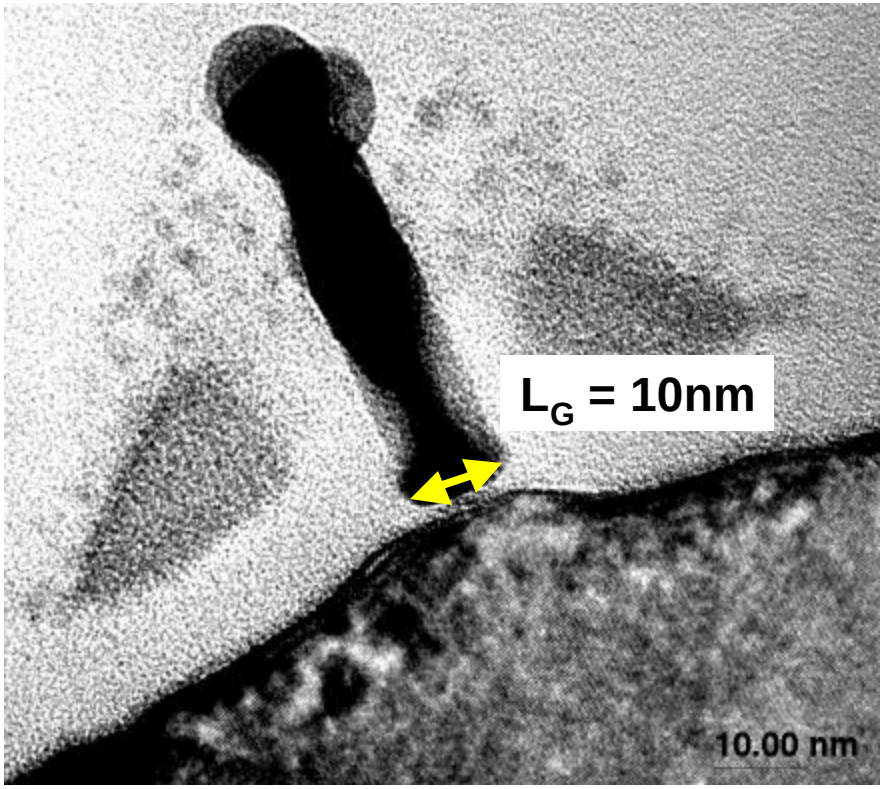
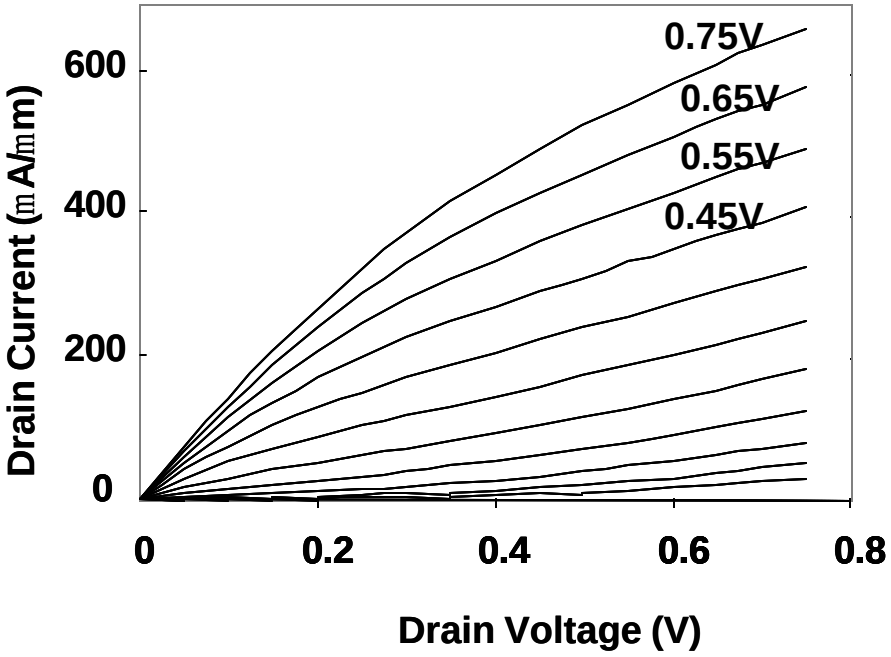
Experimental 10nm Si MOS Transistor





- **10nm transistor still behaves like a transistor !**

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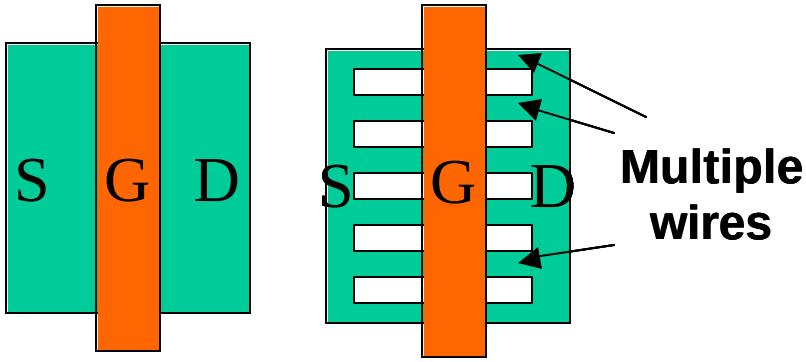
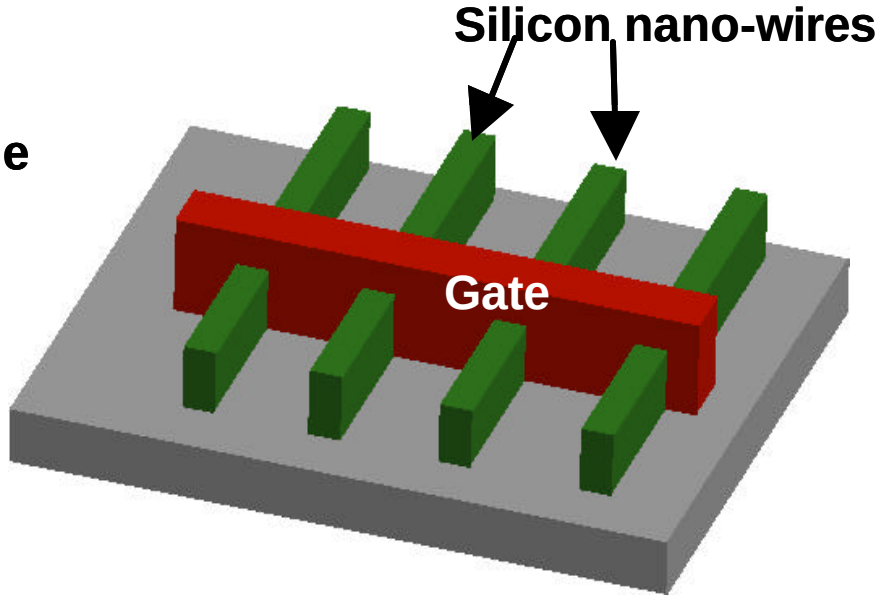
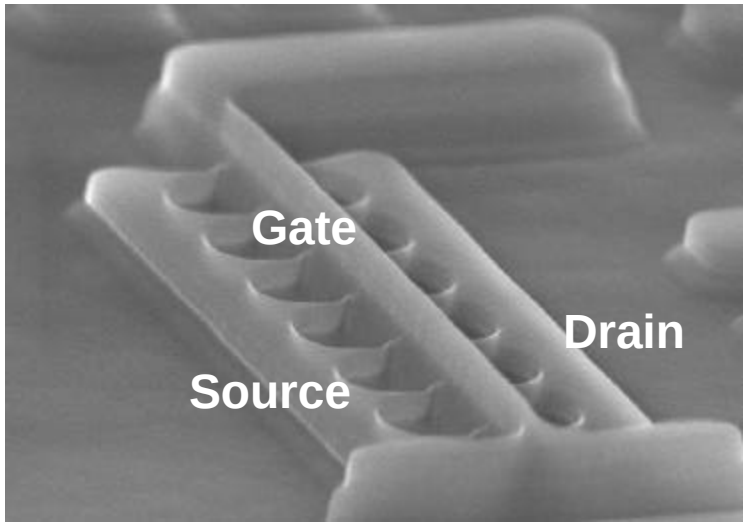
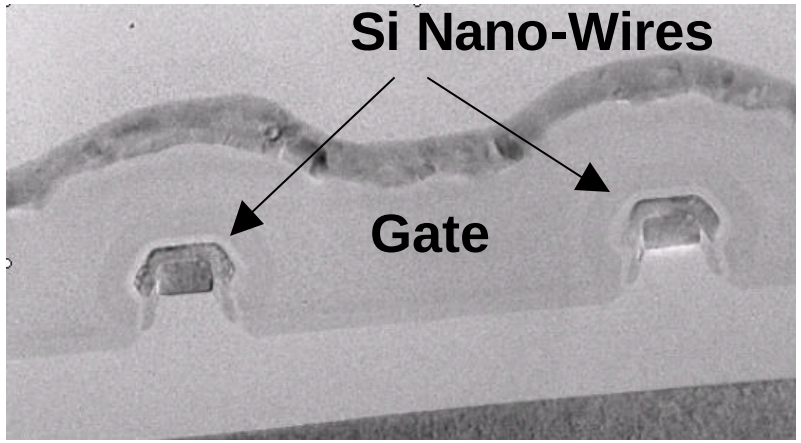
Nano-device Architecture



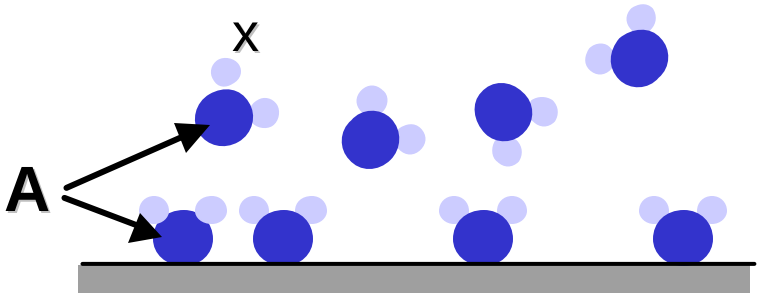
Total Drive Current =
I_d per nanotube/nanowire x no. of tubes/wires



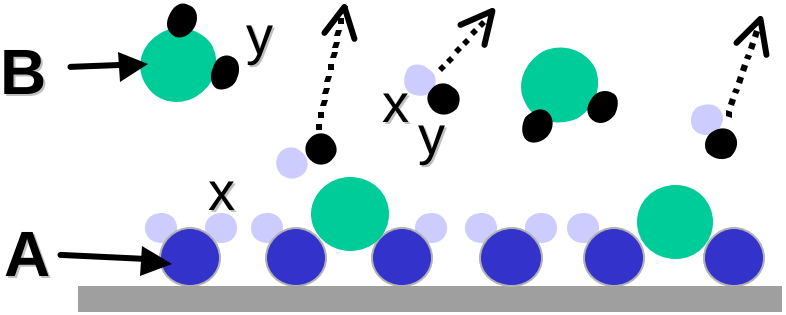




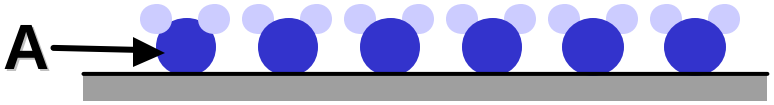
Nanotechnology Example: Crafting Thin Films with Atomic Layer Deposition (ALD)



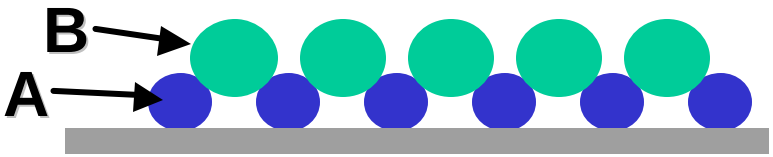
Step 1



Step 3



Step 2



Step 4

ALD: Today's nanotechnology for self-assembly by atomic layer

A Simple Theoretical Model to Predict Si Device Scaling Limit

- **Shannon-von Neumann-Landauer**
  - **Min E_b = KTln2 = 0.017eV (300K)**

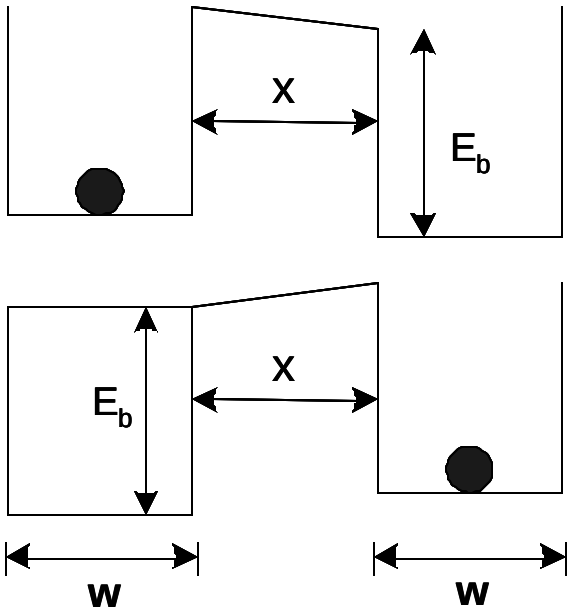
- **Heisenberg Uncertainty Principles**

$$\Delta x \Delta p \geq \hbar$$

$$\Delta E \Delta t \geq \hbar$$

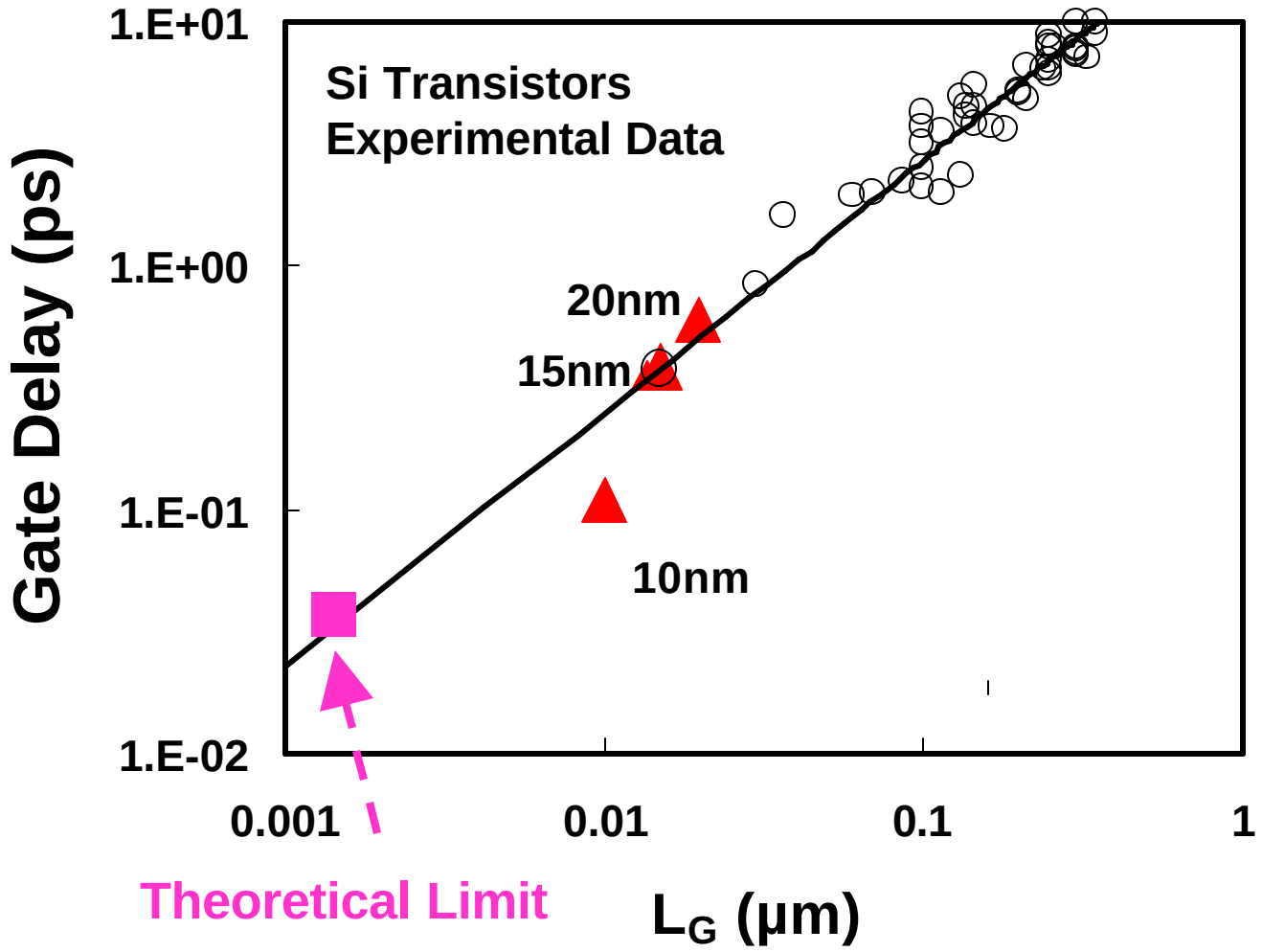
$$x_{\min} = \frac{\hbar}{\Delta p} = \frac{\hbar}{\sqrt{2 m_e E_b}} = \frac{\hbar}{\sqrt{2 m_e kT \ln 2}} = 1.5 nm$$

$$t_{\min} = \frac{\hbar}{\Delta E} = \frac{\hbar}{kT \ln 2} = 0.04\, ps$$



Binary switch in its Simplest form

- **Minimum theoretical size and switching time is 1.5nm and 0.04ps**



- **Theoretical limit falls on experimental trend**
- **Scaled silicon devices are operating like ideal switch (silicon devices close to ideal)**

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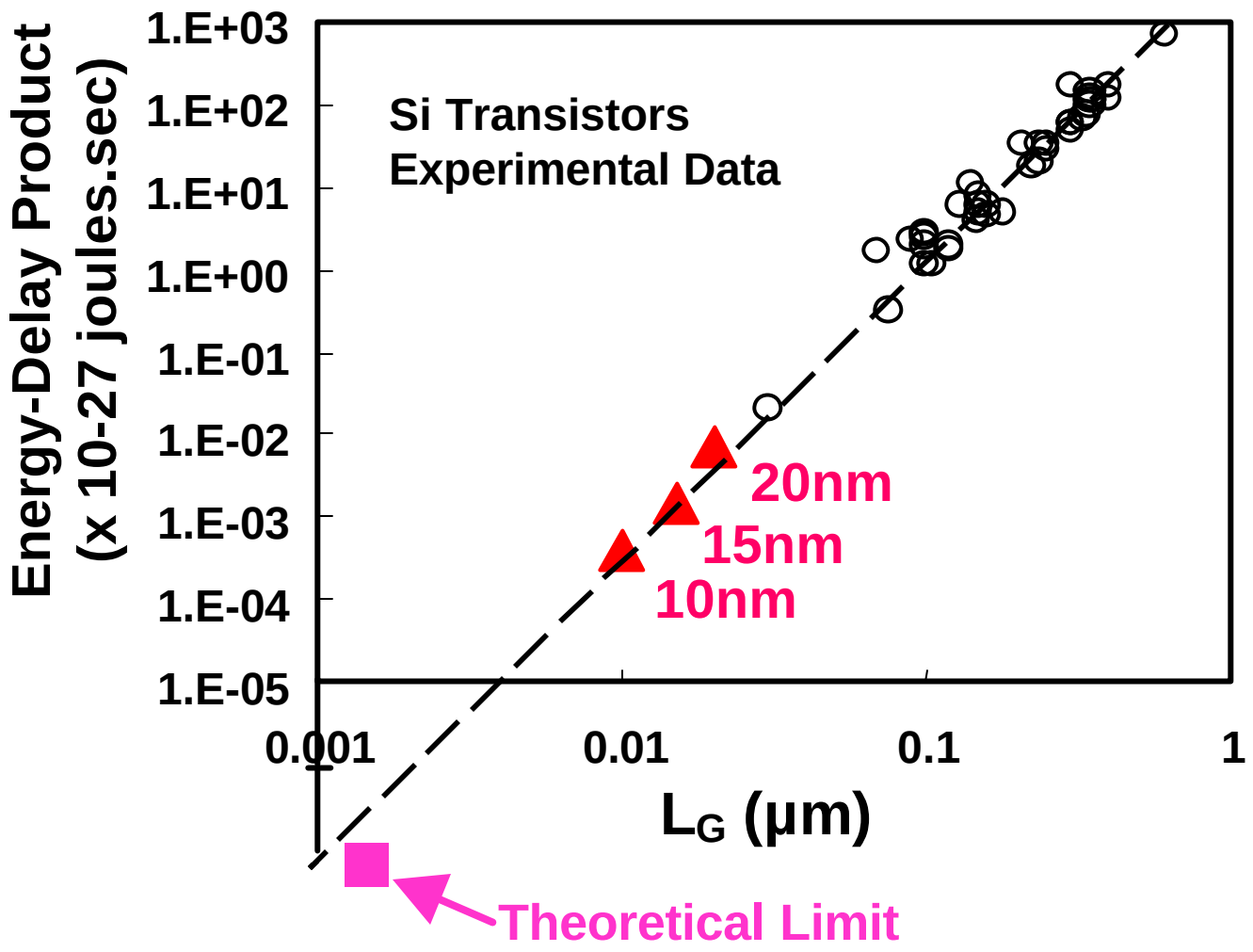

- **Theoretical limit falls on experimental trend**
- **Silicon device is close to ideal switch**

Robert Chau, Intel, Oct 14, 2004

Key Bullets

- **Silicon nano-transistors & Silicon nanotechnology will enable Moore's Law to continue through 2015**
- **Electrical properties of Silicon nano-transistors approaching those of an ideal switch**
- **Need to identify the most promising options for >2015**
  - **Many on-going research programs existing**
  - **Must utilize Silicon technology's foundation**
  - **Semiconductor industry, academia and government need to form close collaboration**

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