
Ultra High-Speed InGaAs Nano-HEMTs

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1st Korea-US Nano Forum

InGaAs Nano HEMTs

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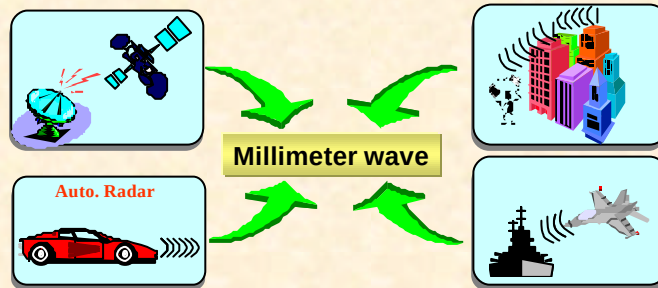
- ❑ **Introduction to InGaAs Nano-HEMTs**
- ❑ **Nano Patterning Process beyond Lithography Limit**
 - Side-wall Gate Process
 - 50nm In_{0.65}GaAs HEMT's
- ❑ **New Triple Shaped Gate Process**
 - 30nm Sidewall Process & Triple Gate Using BCB Planarization
 - 30nm In_{0.7}GaAs HEMT's with high cut-off frequency (f_T)
- ❑ **Application of InGaAs Nano-HEMT Devices**
 - 110GHz Wideband Distributed Amplifier MMIC
 - RTD & HEMT Digital IC : 20Gbps MOBILE
- ❑ **Summary**

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InGaAs Nano HEMTs

Millimeter-Wave/Tera-Hz Technology

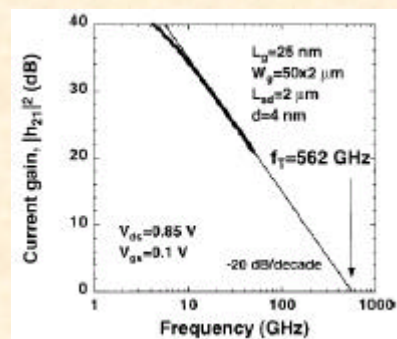
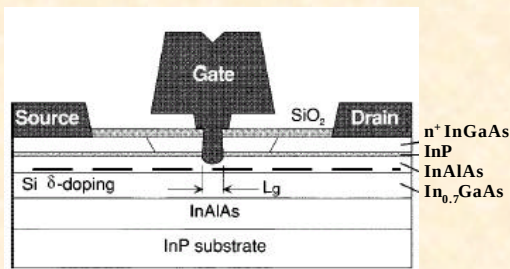
- ◆ Broad Bandwidth $\Rightarrow$ High Speed Data Communication
- ◆ Small Size Antenna $\Rightarrow$ Mobile Communication/Automobile Radar
- ◆ High Resolution Imaging $\Rightarrow$ Biomedical Imaging ($> 100\text{GHz}$)



Demands for High Frequency/High Performance Devices & Circuits

$\Rightarrow$ **Nano-technology enhances the speed of devices & circuits.**
(due to the reduction of carrier transit time)

State-of-the-art InGaAs Nano-HEMT's



CRL-Fujitsu Group's Work (02,EDL)

Gate Length = 25nm

In_{0.7}GaAs Channel

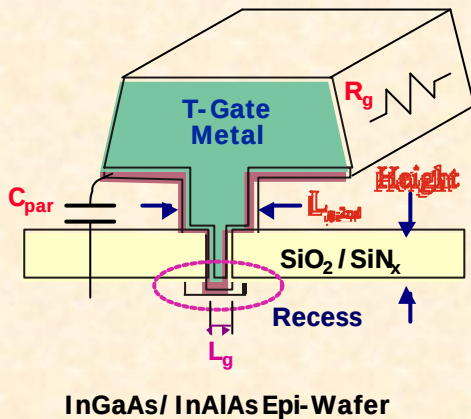
(with $v_{\text{peak}} \sim 3.4 \times 10^7 \text{cm/s}$)

$f_T = 562 \text{GHz}$

(World Record)

* Fabricated by the state-of-the-art E-beam lithography system

How to improve f_T of Nano-HEMT's ?

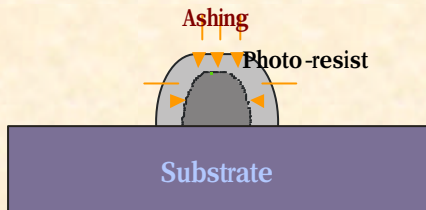


< Cross-section of Nano-HEMT's >

- ❖ L_g Reduction : $L_g < 30\text{nm}$
- ❖ Strained Channel (In_xGaAs)
 - Indium Content > 0.7 for Higher v_{average}
- ❖ Structure for Small Parasitics
 - Reduction of $L_{g,2\text{nd}}$ ($< 100\text{nm}$)
 - Increase of Height ($> 150\text{nm}$) $\rightarrow f_T$ Enhancement
- ❖ Two-Step Recess Etching
 - Damage-Free Condition
- ❖ Structural Stability
 - Wide T-Gate : Small R_g

Nano Patterning beyond Lithography Limit

PR Trimming By Plasma Ashing



Side-wall Process

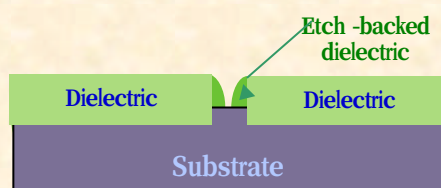
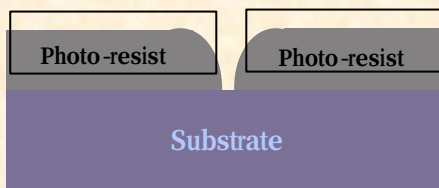
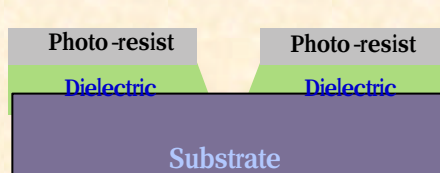


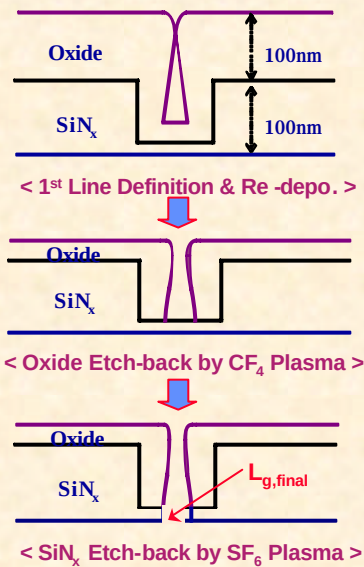
Photo-resist Flow Process



RIE Lag Effect

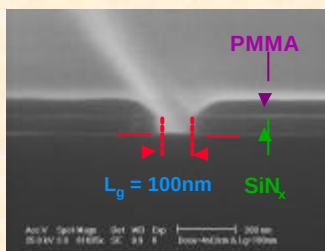


Low-Damage & Reproducible Side-wall Process

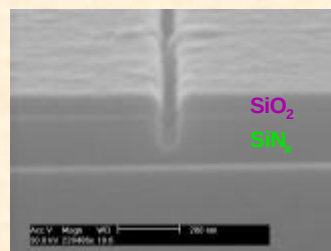


- Two-step Dielectric Etch-back
 - CF_4/O_2 Mixture : Etching SiO_2
 - SF_6/Ar Mixture : Etching the residual SiN_x
 - 1) **Lower Damage** than that of other gas
 - 2) **Etch Selectivity** of SiN_x over SiO_2
 - Typical Selectivity = ~ 20
- $L_{g,\text{final}}$: **Insensitive to over-etch cond.**
- **Low-Damaged & Reproducible**
- $L_{g,\text{final}} = \sim L_{g,\text{initial}} / 2$

Sidewall Process Results : 50nm Line



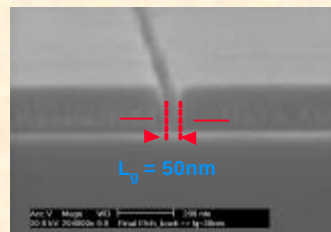
(a) 1st Gate Definition



(c) Etch-Back : On Etching

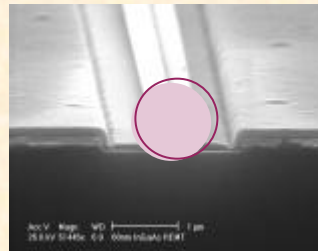
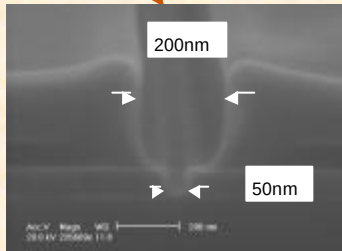
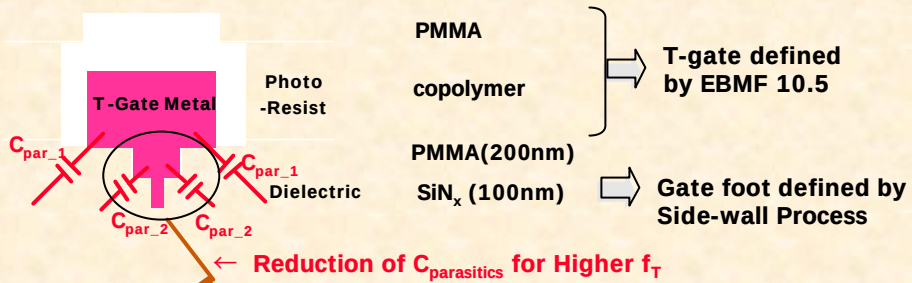


(b) SiO_2 Re-deposition



(d) Final Sidewall Gate

50nm Double Decked T- Gate Fabrication

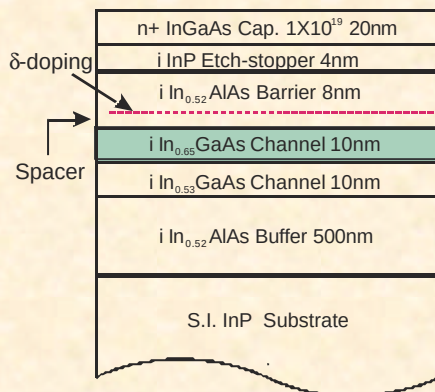


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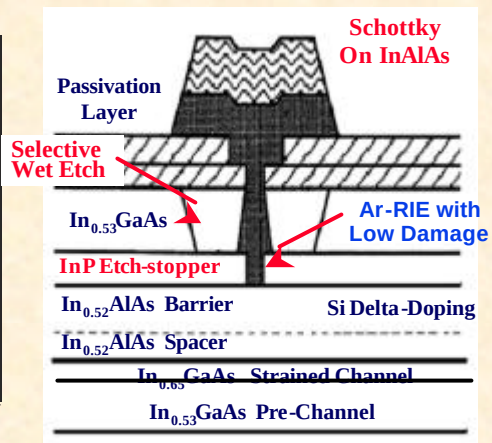
InGaAs Nano HEMTs

Epitaxial Structures for Nano-HEMT Fabrication

< Epitaxial Structure >



< Cross-Section of Nano-HEMT >



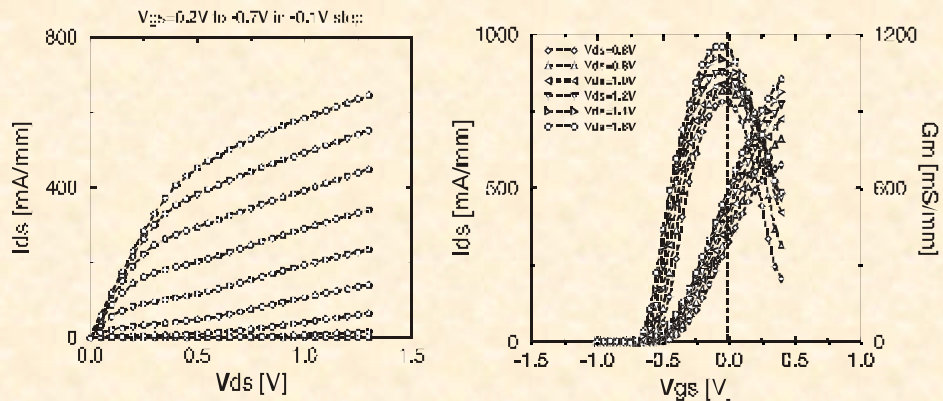
$$n_s = 3 \times 10^{12} / \text{cm}^2, \quad m_{n, \text{hall}} = 10,300 \text{ cm}^2 / \text{V-s}$$

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InGaAs Nano HEMTs

50nm InGaAs Nano-HEMT : DC Characteristics

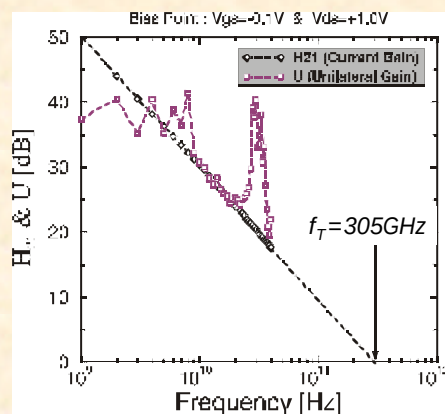
< $L_g = 50\text{nm}$ & 65% Strained InGaAs Channel >



$\Rightarrow V_{th} = -0.6\text{V}$ & $G_{m,max} = 1.07\text{S/mm}$ @ $V_{ds} = 1.0\text{V}$

50nm InGaAs Nano-HEMT: Microwave Characteristics

- Bias Point : Maximum Transconductance Condition -

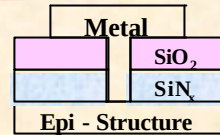


$\Rightarrow f_T = 305\text{GHz}$ & $f_{max} = 302\text{GHz}$

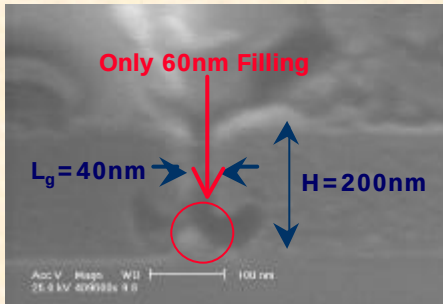
InGaAs Nano-HEMT's : Metal Filling Issue

High Performance Nano-HEMTs

- $L_g \downarrow$, T-Gate Aspect Ratio $\uparrow$ (For Small $C_{parasitics}$)
- metal filling of fine line with high A-R needed.

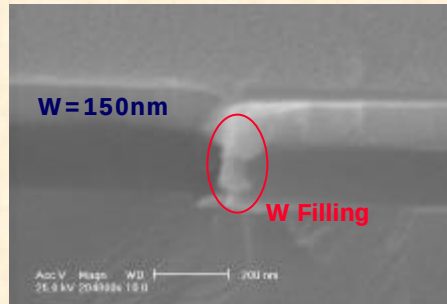


< Gate Filling By E-Beam Evaporation > < Gate Filling By W-Sputtering >



Aspect Ratio (H/L_g) = 5

Not Filled After 50nm Evaporation

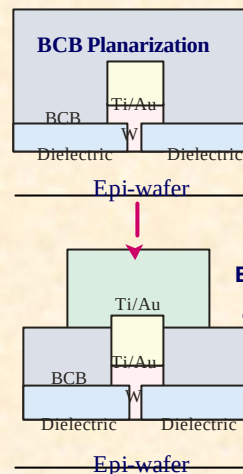
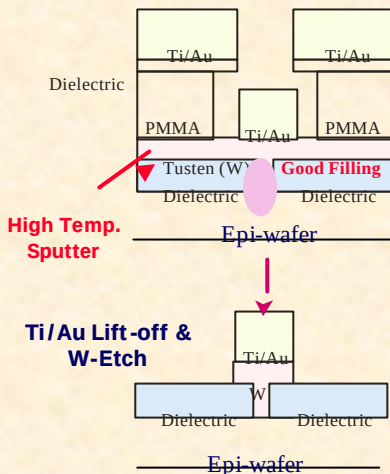


Good Gate Metal Filling

W : Good Thermal Reliability

T-Gate Process for 30nm InGaAs HEMT's

High Temp. Sputter : Problem in Lift-off → Metal Etch Process

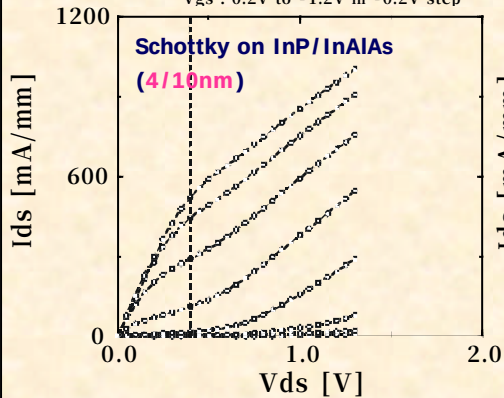


< New Triple Gate Process Using High Temp. Sputter & BCB Planarization >

30nm In_{0.7}GaAs HEMT's : DC I-V

< L_{side-etch} = 50nm & No InP Etch >

V_{gs} : 0.2V to -1.2V in -0.2V step



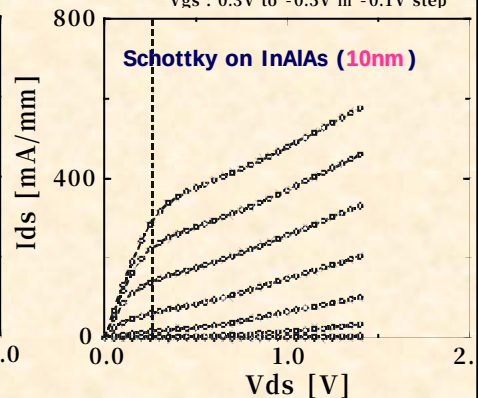
=> V_{th} = -0.85V & G_{m,max} = 1.75S/mm

=> High Short channel effect

G_m/G_{ds} = 3.89 @ G_{m,max} Bias Point

< L_{side-etch} = 50nm & InP Etch >

V_{gs} : 0.3V to -0.5V in -0.1V step



=> V_{th} = -0.3V & G_{m,max} = 1.69S/mm

=> Low Short channel effect

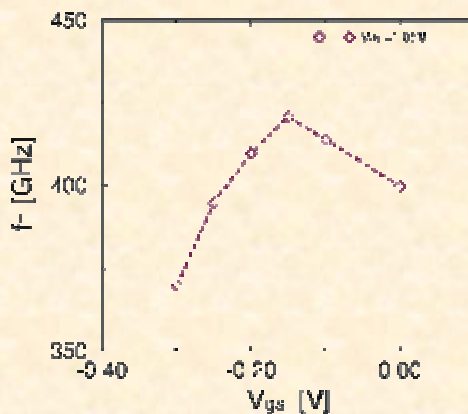
G_m/G_{ds} = 10.6 @ G_{m,max} Bias Point

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InGaAs Nano HEMTs

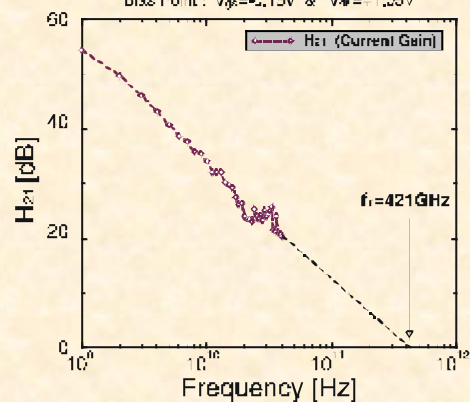
RF Characteristics of 30nm In_{0.7}GaAs HEMT's

< f_T versus Gate Bias >



< Best f_T Characteristics >

Bias Point : V_{gs} = -0.15V & V_{ds} = -1.05V

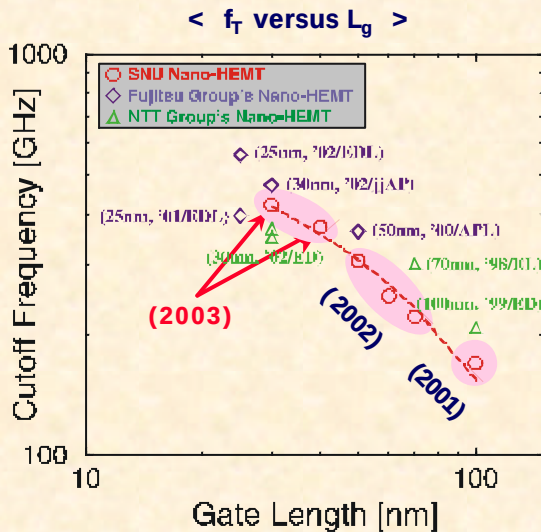


→ f_T = 421GHz at V_{gs} / V_{ds} = -0.15 / 1.05V

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InGaAs Nano HEMTs

Performances of SNU InP Nano-HEMT's



$$f_T = \frac{1}{2\pi} \cdot \frac{v_{sat}}{L_{G,eff}}$$

L_G reduction

⇒ decrease of $\tau_{transit}$

⇒ increase of f_T

SNU InGaAs Nano-HEMT

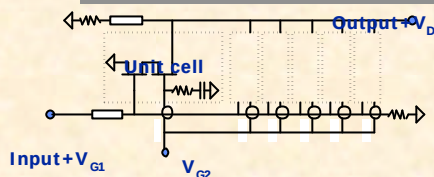
→ $f_T = 250\text{GHz}$ for $L_g = 60\text{nm}$

→ $f_T = 305\text{GHz}$ for $L_g = 50\text{nm}$

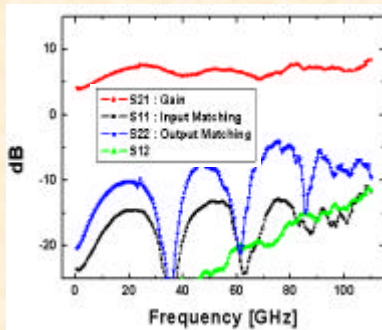
→ $f_T = 371\text{GHz}$ for $L_g = 40\text{nm}$

⇒ $f_T = 421\text{GHz}$ for $L_g = 30\text{nm}$

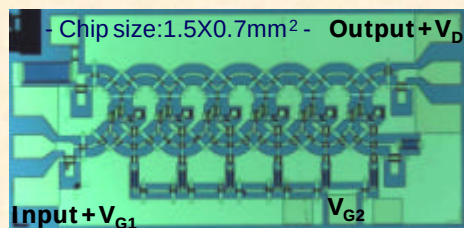
Over 110GHz Broadband Distributed Amplifier



< Schematic of distributed amplifier >



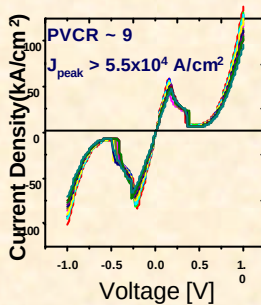
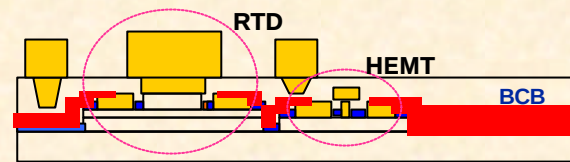
< Measured S-parameter >



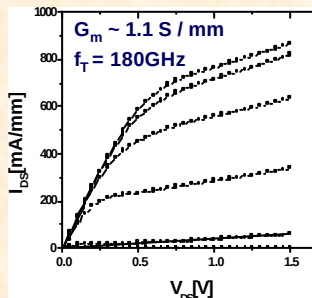
< Photograph of distributed amplifier >

- Broadband distributed amplifier with 60nm InGaAs Nano-HEMT
- The average gain at **1~110GHz** is about **6.6 dB**.
- $S_{11} < -11\text{ dB}$, $S_{22} < -4\text{ dB}$

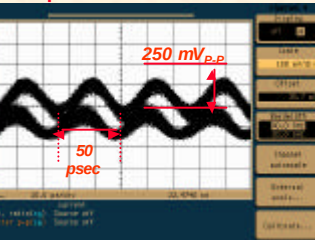
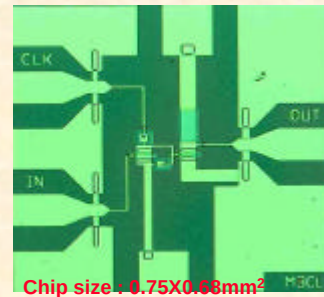
RTD & HEMT Digital IC – 20Gbps MOBILE



< RTD I-V Curve >



< HEMT I-V Curve : $L_g=100\text{nm}$ >



20Gbps $2^{31}-1$ PRBS Output Signal

Summary

- ❑ Nano Patterning Method beyond Lithography Limit
 - Sidewall Process / Resist Flowing / Sloped Etch By RIE-Lag
- ❑ 30nm $\text{In}_{0.7}\text{GaAs}$ Nano-HEMT
 - Sidewall Process + Triple Gate Process Using BCB Planarization
 - $G_{m,\text{max}} = 1.75\text{S/mm}$ & $f_T = 421\text{GHz}$
- ❑ Application of Developed InGaAs Nano-HEMT Device
 - 110GHz Wideband Distributed Amplifier (DA) MMIC : B-W > 110GHz
 - MOBILE IC based on RTD & HEMT Integration > 20Gbps
- ❑ In future, the high speed characteristics of InGaAs nano-HEMT are to be enhanced with nano-technology [reduction of gate length], and ultra-high-speed ICs are to be implemented with nano-HEMTs.