# Nanoscale Si-based Nonvolatile Memories

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## ABSTRACT

In the conventional floating gate (FG) type nonvolatile memories (NVMs), the relatively thick (7-12nm) tunnel oxide layer is employed guarantee retention characteristics. A thick tunnel oxide also eases the process control in the oxide growth, thus making floating gate technology a popular choice in the semiconductor industry [1]. However, it was reported that floating gate type memory is related in low yield due to the discharge of stored negative charges through any porous in thnnel oxide under floating gate as the thickness of tunnel oxide layer becomes thinner and thinner [2]. This problem is related with high conductivity of floating gate.

Nano-crystals [3] and SONOS (silicon-oxide-nitride-oxide-silicon) memories [4] using discrete memory nodes were widely studied to overcome the problems of the conventional FG NVMs. Nano-crystal memories have been worked as a fusion of the existing flash memory technology and rapidly growing nanotechnology [5]. On the other hand, , the charge leakage from nitride layer to tunnel oxide is greatly reduced, since the stored charge in silicon nitride of SONOS memory is localized in the traps [6, 7]. The fabrication process of SONOS memory device is also compatible with high density scaled CMOS technology. For these reasons, interest in SONOS technology for next generation nonvolatile memory applications (NVMAs) has been more stimulated by the possible application to portable telecommunication devices which demand lower programming voltage, lower power consumption and higher packing density.

We report characteristics of SONOS memories with short channel widths and lengths (30 nm and above) fabricated on SOI substrates using electron-beam lithography. The devices show attractive endurance and programming properties, achieve a size-independent memory window, and achieve good endurance characteristics. The large density of interface states available for trapping allows these structures to function to length scales as small as 46 nm with reproducible characteristics. The smallest memory structures tested in this effort, ~30 nm, show the existence of the trapped charge memory effect.

**References**

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