

Silicon Nano-transistors and Silicon Nanotechnology for High-Performance Logic Applications

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ABSTRACT

The tremendous effort put forth in scaling silicon transistors has led to very high levels of integration and extremely high performance in logic products. Commercial microprocessors have grown in complexity starting from several thousand transistors in the early 1970's all the way to more than 100 million transistors in microprocessors manufactured today. This trend has followed the Moore's Law which states that the number of transistors doubles about every 18 months. In order to facilitate this trend, silicon transistor performance and energy-delay product have continued to improve. Towards this, the silicon transistor physical gate length (L_G) has been scaled by approximately 30% every generation, with the pace quickening in recent technologies. Current mainstream production at the 130nm technology node actually produces silicon CMOS devices with physical L_G of about 70nm, with 50nm devices in the 90nm technology node expected to be in production before end of 2003. The L_G is expected to reach 15nm by the end of this decade and 10nm early next decade. Research silicon transistors with physical gate length of 20nm, 15nm and even 10nm have already been demonstrated in laboratories. Considering that an influenza virus is only 100nm, the size of silicon transistors produced today in factories and research laboratories are already much smaller than a common virus. Thus the size of silicon transistors produced today is already in the "nano-regime" and should be termed "silicon nano-transistors". In this presentation I will i) show the scaling trends in the silicon industry, ii) show some examples of Si nano-transistors with 20nm, 15nm and 10nm physical gate lengths, iii) describe a new transistor architecture that is useful for silicon nano-transistors as well as other electronic devices such as nano-wire transistors and nano-tube transistors, iv) describe several key silicon nanotechnologies that are required for continual silicon transistor scaling, and v) discuss a first-order model which predicts the theoretical fundamental scaling limit of Si nano-transistor to be at about 1.5nm.