Ultra High-Speed InGaAs nano-HEMT's

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ABSTRACT

InP-based High Electron Mobility Transistor (HEMT) is the fastest transistor among the all three-terminal semiconductor devices at present and must be the key device for future ultra high-speed electronic systems. To obtain a higher cutoff frequency (f_T), many experimental works have been made to reduce the gate length and to achieve the record highest f_T. The Fujitsu group yielded the best f_T results recently. They have developed several fabrication techniques such as 25nm T-gate process with high bottom-to-top aspect ratio and two-step recess etching and obtained an ultra high f_T of 562GHz.

Generally, the difficulty to define a very fine line results from the resolution of electron-beam lithography system. To overcome this limitation, the sidewall process can be utilized as cost-effective alternatives. In the conventional method with single sidewall dielectric layer, it's difficult to control the final length reproducibly because there exist some process ambiguities such as the exact thickness of the re-deposited dielectric layer and the etch-back time. We employed two different dielectric layers of SiN_x and SiO_2, and the proper selection of etching gas was done in the etch-back step. Using the newly developed sidewall process, we could easily obtain much finer lines such as 30nm. To increase the cutoff frequency further, it's also necessary to form the T-shaped gate structure with high bottom-to-top aspect ratio so that parasitic capacitances incorporated with T-shaped gate and dielectric layer can be effectively suppressed. For this purpose, double deck-shaped triple gate process was employed.

Heightening the bottom gate foot brings another process problem of metal filling in narrow gate line with high aspect ratio. Typically, 30nm gate line with aspect ratio of above 3 was not fully filled with conventional e-gun evaporation method. To resolve this metal filling problem, we optimized tungsten metal sputtering process in order to ensure good metal filling. The process variables, such as substrate temperature and the distance between metal target and substrate, were carefully considered. In order to fabricate 30nm double deck-shaped T-gate nano-HEMT, we developed the new triple gate process with BCB planarization layer. The middle gate part was made by defining 100nm-scale Ti/Au pattern and etching the unnecessary sputtered tungsten masked by this pattern. Finally the upper wide gate head was formed on the top of planarized and etched BCB layer. With the proposed triple gate process, ultra-high-speed 30nm $In_{0.7}GaAs$ HEMT could be successfully fabricated with $G_{m,max}$ of 1.6S/mm and f_T of 421GHz, without the aid of state-of-the-art electron beam lithography system. Since the developed triple gate process is much more effective in metal filling and offers better structural stability, it can be directly applicable to the fabrication of future nano-HEMT's with gate length less than 30nm.