Major Changes

None

What Have You Accomplished So Far?

I have been designing and writing an FFT unit to perform a Fast Fourier Transform. I’ve spent a lot more time being more independent in designing the units as compared to the beginning where I was working on sorting. Even as I get more comfortable with designing and programming, that just means that I am more able to do more features. We planned the initial dataflow of the unit, and came to terms with a roughly efficient design after my initial one.

I’ve also been doing some side research surveys on a combination of verification and “ease of coding”. Designing and writing such low level code is an extraordinarily laborious task. There’s a reason why realistically only very large manufacturers with deep pockets can produce sophisticated and optimized processors. Work in academia, and smaller more niche manufacturers has a hard time being able to produce as optimized processors due more to time spent on implementation, rather than design. Most time in implementation is spent due to debugging. So, I’ve been interested in seeing what has been done with regards to this. Both in terms of language design, and the verification side of things. This is focused more on augmentations to Verilog/VHDL which are heavily entrenched. There exist many other languages for hardware design, but never (and probably never will without the support of a very large manufacturer) see mass adoption primarily due to the entrenchment of Verilog/VHDL.

Meeting Your Milestone

I’ve gone a lot farther than what I expected in my milestones, and I feel like I’m at the 150% level right now.

Surprises

None.

Revisions to Your 15-400 Milestone

None

Resources Needed

None