ADVANCED IC PACKAGING USING SILICON INTERCONNECT FABRIC

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Abstract

The ever-growing demand for data-bandwidth is pushing boundaries of traditional IC packaging technologies. Moreover, the slow-down of Moore's law has accelerated a paradigm shift in packaging technologies, assembly techniques, and heterogeneous integration solutions for system scaling. The Silicon-Interconnect Fabric (Si-IF) technology is a silicon-based, package-less, fine-pitch, highly scalable, heterogeneous integration platform that uses unpackaged dielets to be assembled at small inter-dielet spacings (≤100 μm) using fine-pitch (≤10 μm) interconnects. These fine-pitch interconnects are made possible using a solder-less direct metal-metal (gold-gold and copper-copper) thermal compression bonding that have low specific contact resistance of ≤0.7 Ω-μm^2. Therefore, this integration scheme allows for a large number of parallel, short, on-chip like data-links (≤500 μm) between dielets. As a result, simple IOs can transfer data between dies using a Simple Universal Parallel intERface for chips (SuperCHIPS) at low latency (<30 ps), low energy per bit (≤0.03 pJ/b), and high data- rates (up to 10 Gbps/link), corresponding to an aggregate bandwidth of ≥8 Tbps/mm. These benefits were experimentally demonstrated to provide 8-30X reduction in latency, 5-90X improvement in data-bandwidth, and 5-40X improvement in energy per bit compared to existing integration schemes.