

# Applications of 2D Materials in Future CMOS Nodes

**Steven J. Koester**

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*Electrical and Computer Engineering Department  
University of Minnesota*



# University of Minnesota

- The University of Minnesota - Twin Cities is public research university located in Minneapolis and Saint Paul, MN.
- It has the 9<sup>th</sup> largest main campus student body in the United States, with over 52,000 students at the start of the 2021–22 academic year.



# Minnesota Nano Center

- The Minnesota Nano Center (MNC) is a state-of-the-art, open-access facility for advanced research and education in micro- and nano-scale technology:

<https://cse.umn.edu/mnc>

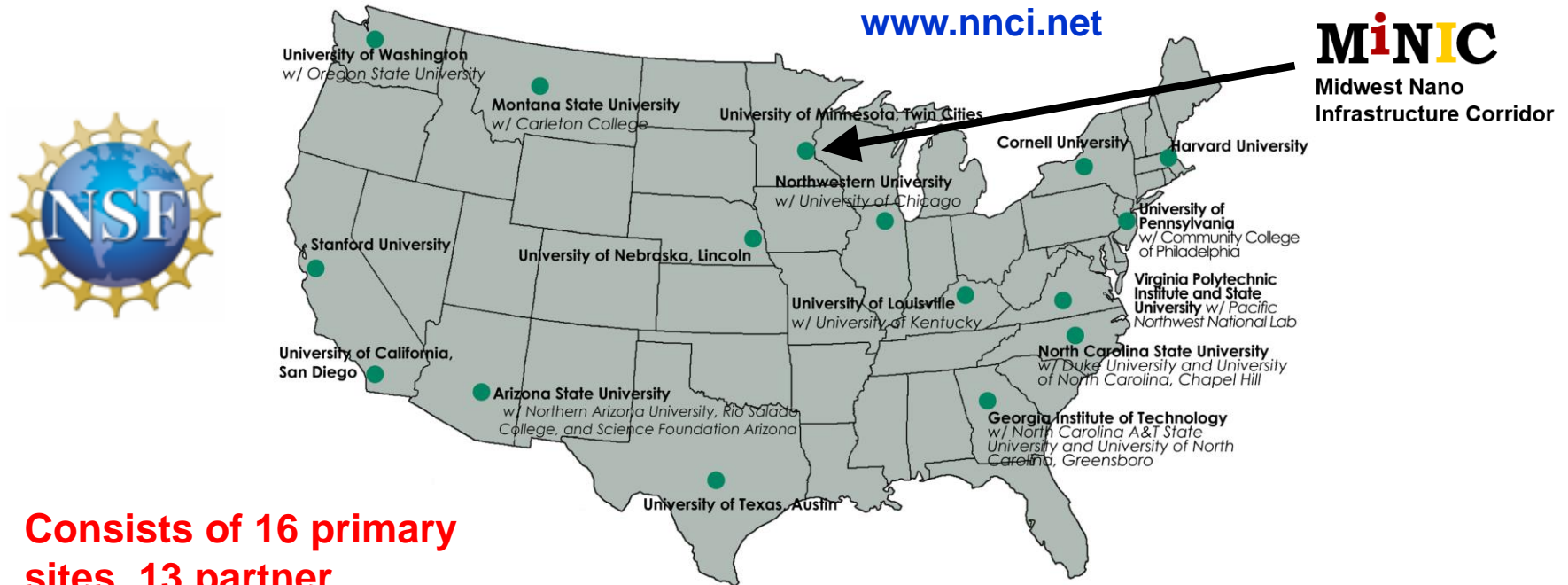


- **MNC is open to any qualified user, with significant use from industry and other institutions.**
- **Annually serves ~400 total users, ~140 external and ~60 industry.**



# NNCI

- MNC is part of one node of the National Nanotechnology Coordinated Infrastructure (NNCI), a network of university nanofabrication and characterization facilities across the US:



- **Consists of 16 primary sites, 13 partner institutions, and 69 facilities in total.**
- **Supports > 2000 individual nanofab tools.**

- **NSF has provided \$165M in support between 2015-2025.**

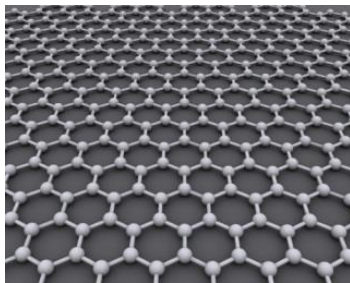




# 2D Materials

- 2D materials are crystalline solids where the in-plane bonding is much stronger than in the out-of-plane direction. Can exist as single monolayers. Span a range of band gaps from 0 to 6 eV.

Graphene



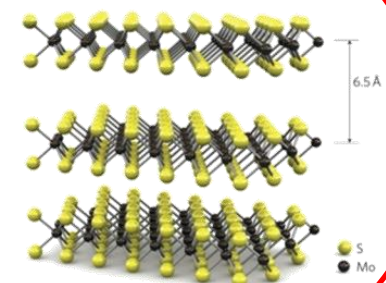
$\mu \sim 10,000 \text{ cm}^2/\text{Vs}$

Black phosphorus

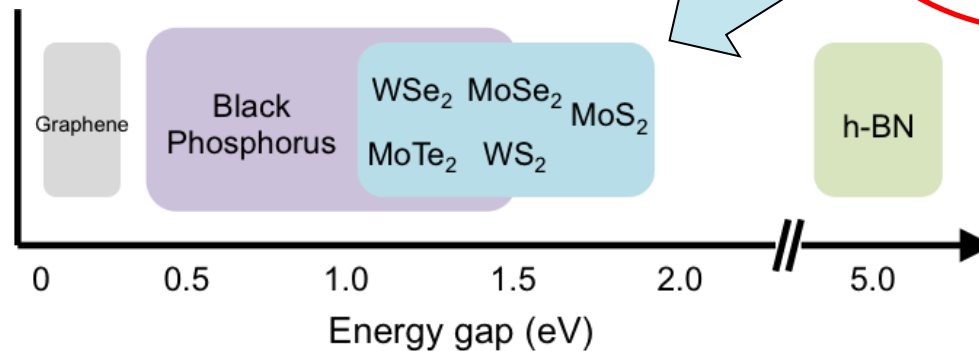


$\mu \sim 1000 \text{ cm}^2/\text{Vs}$

TMDCs ( $\text{MX}_2$ )



$\mu \sim 100 \text{ cm}^2/\text{Vs}$

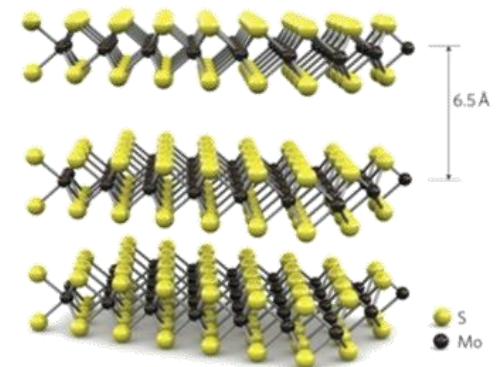
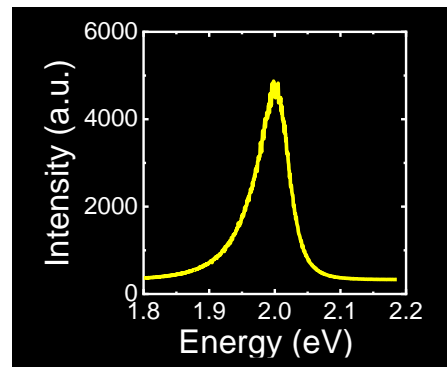
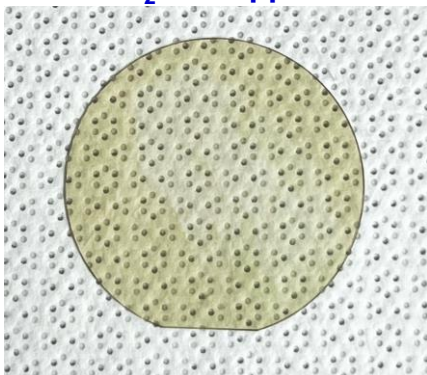


- TMDCs have emerged as front-runners for use in future CMOS.**

# Advantages of TMDCs

- TMDCs meet the necessary criteria for being a candidate for end-of-roadmap CMOS:
  - Scalable to monolayer thickness (where  $\mu$  can beat Si).
  - Electron and hole effective mass and mobilities are similar.
  - Capable of meeting IRDS off-current targets (due to  $E_G \sim 1\text{-}2$  eV).
  - Stable in atmosphere and under high processing temperatures.
  - Capable of large-area (up to 300-mm) growth with high-degree of uniformity over an entire wafer.

WS<sub>2</sub> on sapphire

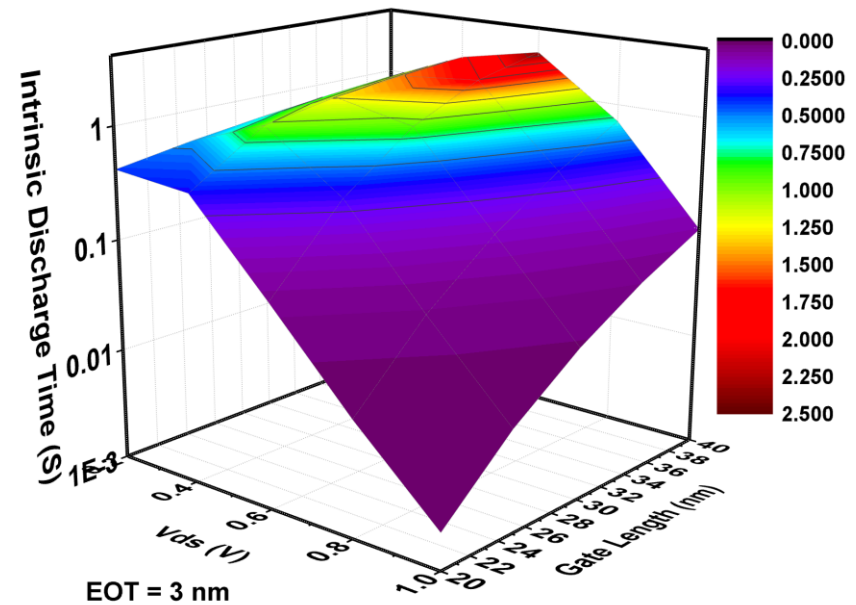
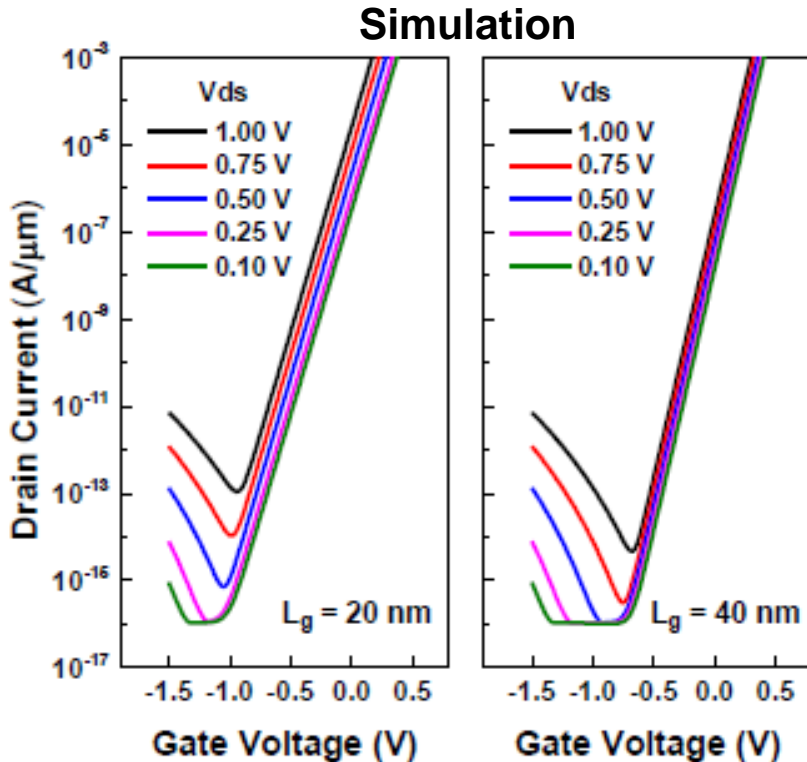
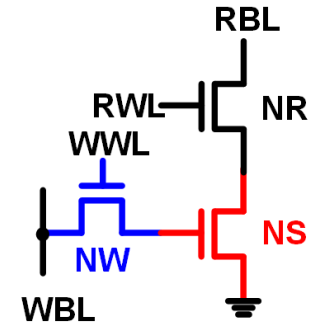


# TMDCs for Dynamic Memories

- TMDCs are ideal for embedded DRAM due to the extremely-low leakage currents possible:

C. Kshirsagar...S. J. Koester, et al., DRC, 2014.

Results from large band gap ( $E_G \sim 2$  eV) and heavy effective mass.

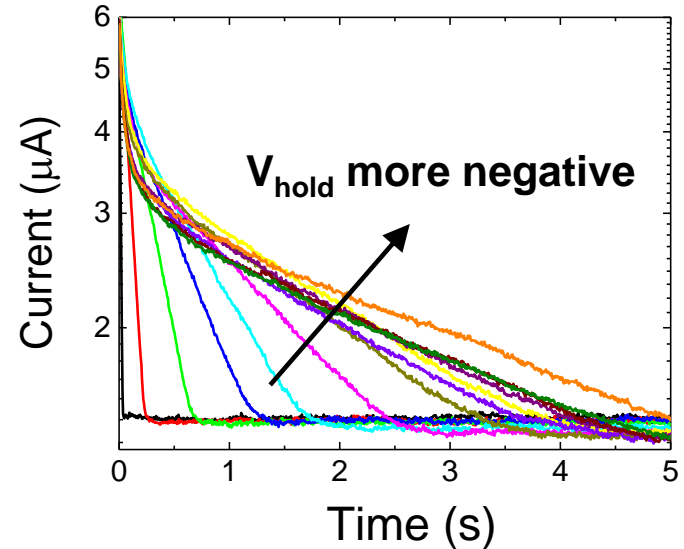
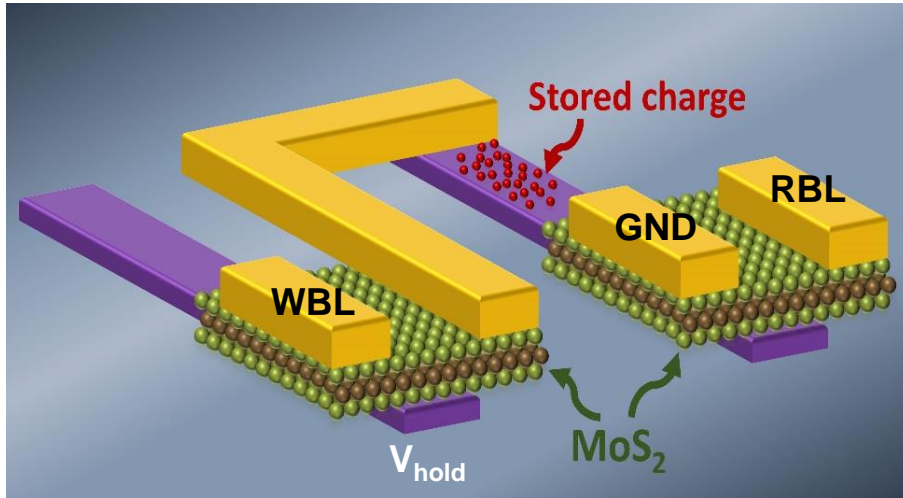


- Device simulations show sub-fA leakage currents possible for  $\text{MoS}_2$ . When used in a 3T “gain cell”, can achieve retention times  $> 1$  sec.

# TMDCs for Dynamic Memories

- Demonstrated 2T DRAM using few-layer MoS<sub>2</sub>:

C. Kshirsagar...S. J. Koester, et al., *ACS Nano* 10, 8457 (2016).



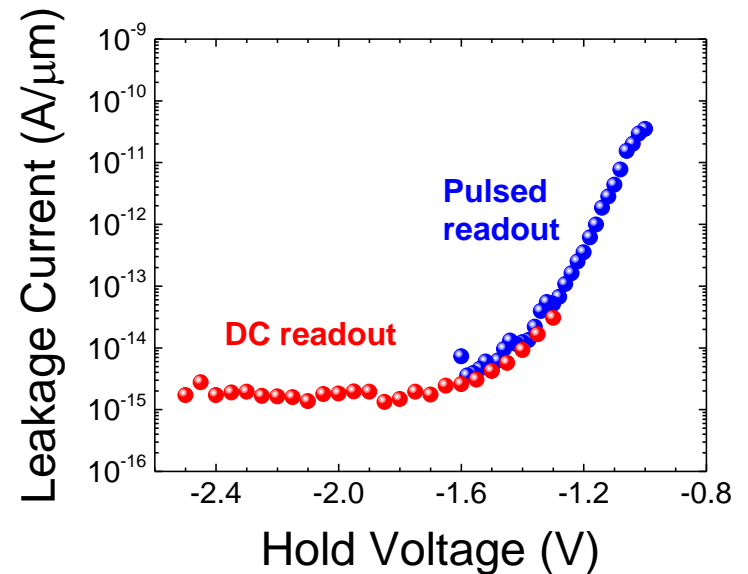
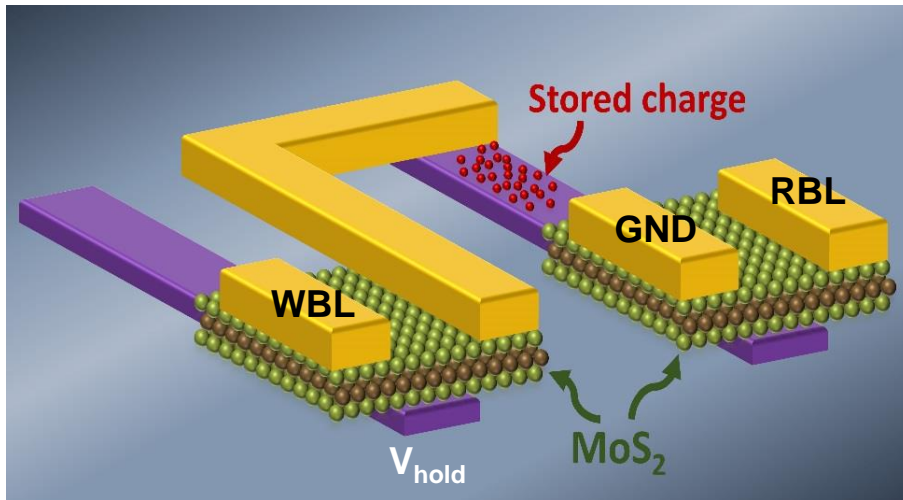
- **Extracted characteristic retention time as a function of gate voltage on access transistor (V<sub>hold</sub>).**
- **Retention time can then be converted into an equivalent leakage current, to understand leakage limitations of MoS<sub>2</sub>.**



# TMDCs for Dynamic Memories

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C. Kshirsagar...S. J. Koester, et al., *ACS Nano* 10, 8457 (2016).

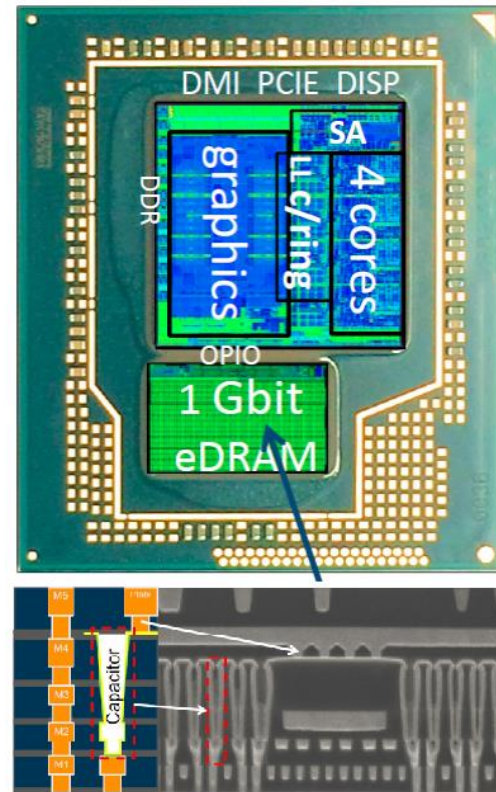
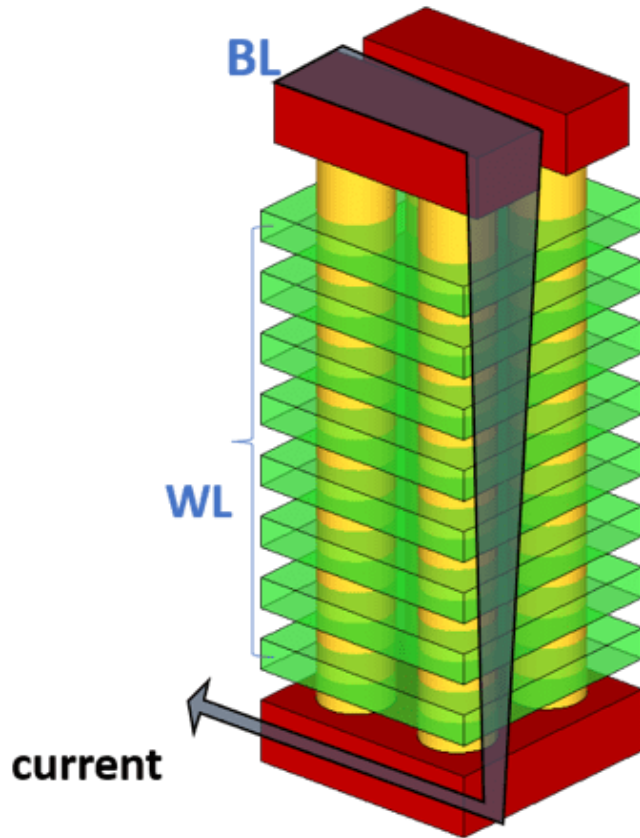


- **Demonstrated 2T memories with equivalent leakage currents approaching 1 fA/μm.**
- **Several orders of magnitude improvement possible using single-layer MoS<sub>2</sub> and optimizing design.**

# Future DRAM Applications

- 2D semiconductors have potential for use in 3D DRAM or ultra-scaled embedded DRAMs:

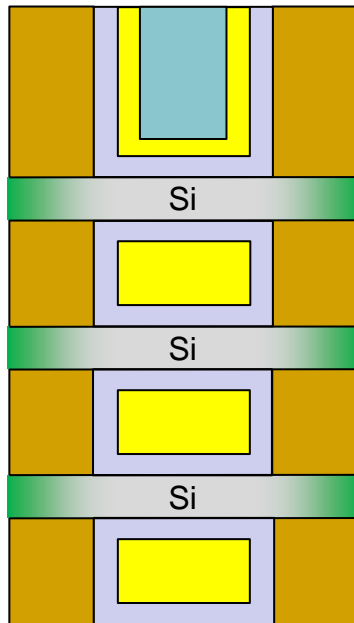
Source: SemiconductorEngineering



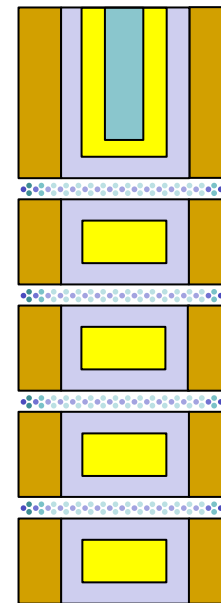
# 2D Nano-Sheet MOSFETs

- 2D materials are being considered for sub-1-nm node CMOS. These devices will be nanosheet FETs:

Si NS-FET (1-nm node)



2D NS-FET (0.7-nm node)

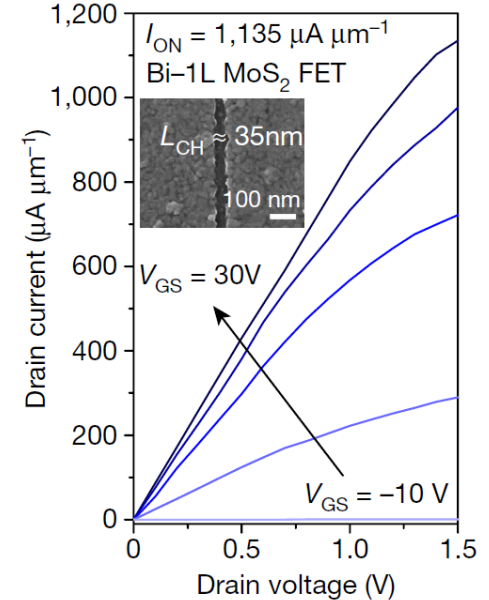
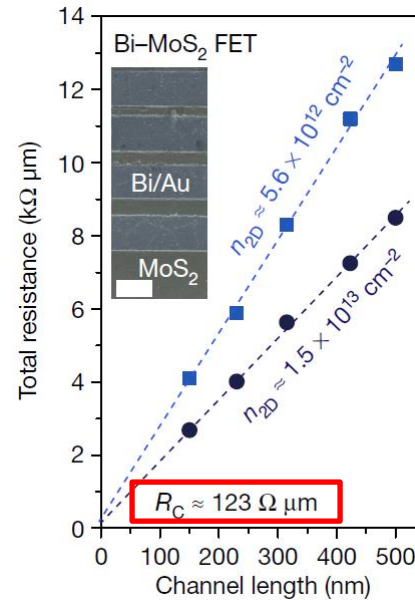
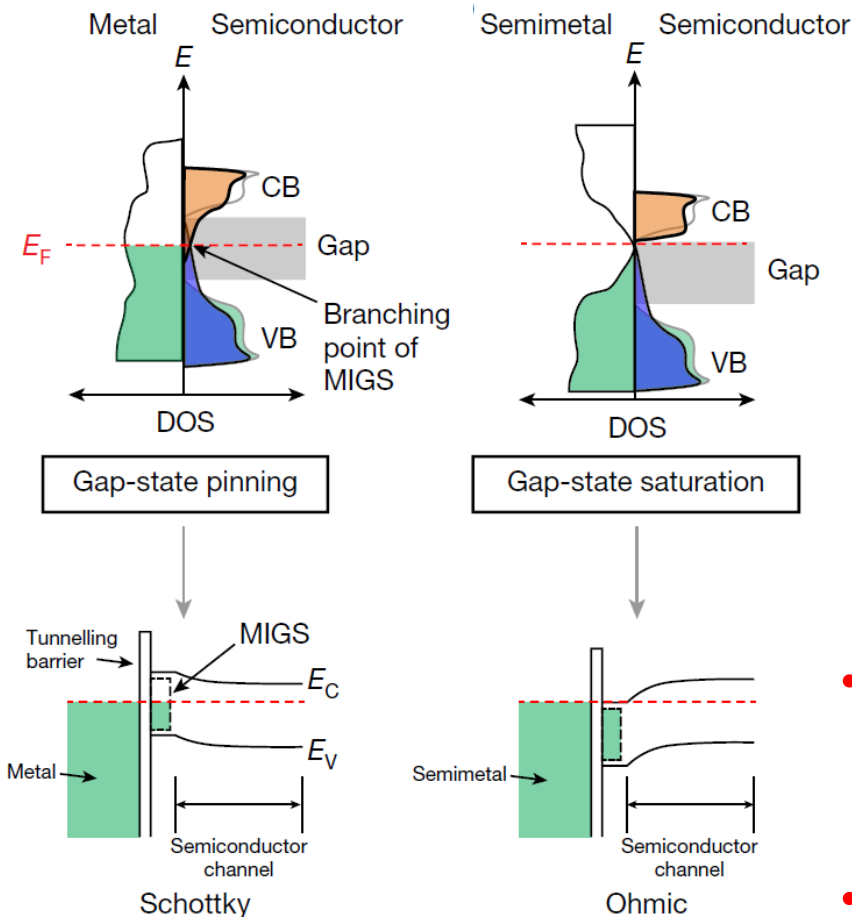


- One key challenge is need for low contact resistance to meet IRDS targets for on-current ( $R_C \sim 60 \Omega\text{-}\mu\text{m}$  needed).**

# Semi-Metallic Contacts to 2D Semiconductors

- Breakthrough reported in 2021 → semi-metallic contacts to MoS<sub>2</sub> can overcome Fermi-level pinning that limits contact resistance:

P.-C. Shen, et al., *Nature*, 593, 211 (2021).



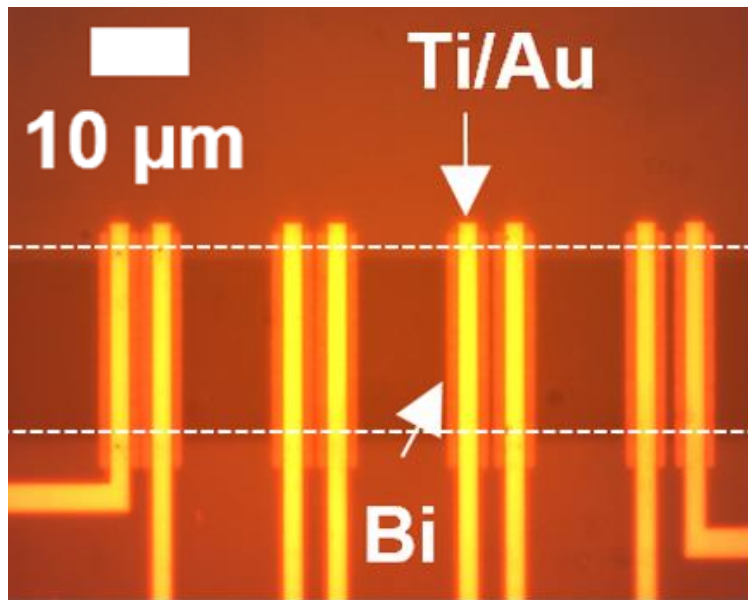
- Semi-metallic contacts have low density of states near Fermi level, mitigating the effect of MIGS.**
- Bi has lowest barrier height, followed by Sb and As.**



# Our Work on Semi-Metallic Contacts to WS<sub>2</sub>

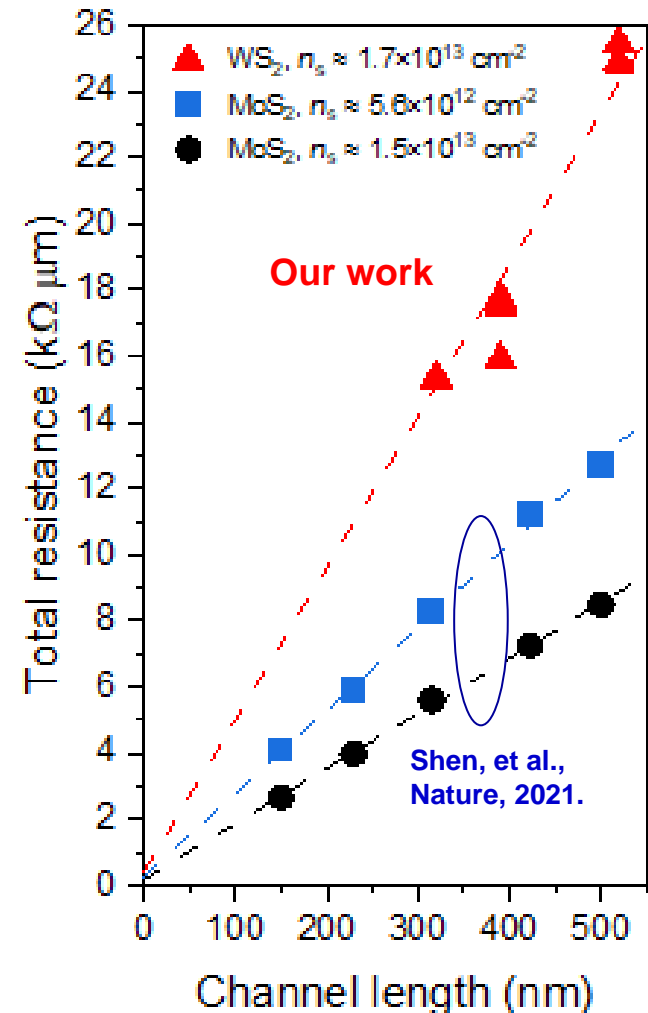
- We have been investigating semi-metallic contacts to WS<sub>2</sub>, which is more promising for CMOS:

L. Jin and S. J. Koester, IEEE EDL 43, 639-642 (2022).



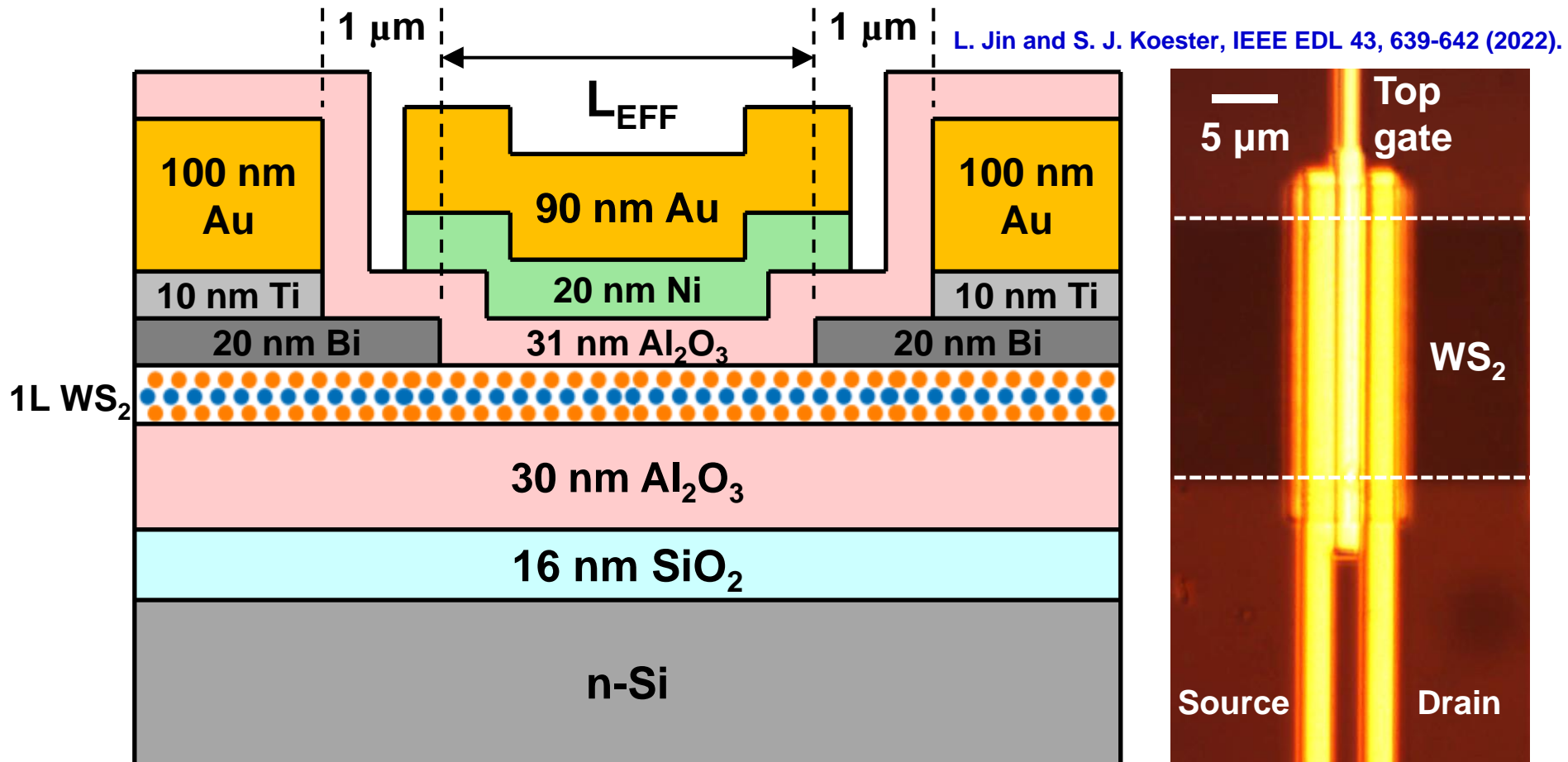
- Demonstrated contact resistance as low as of  $R_C = 220 \Omega\text{-}\mu\text{m}$ , consistent with results of Shen, et al. on MoS<sub>2</sub>.**

Work funded by Intel.



# *WS<sub>2</sub> MOSFETs with Bi Contacts*

- Fabricated WS<sub>2</sub> MOSFETs with semi-metallic Bi contacts:



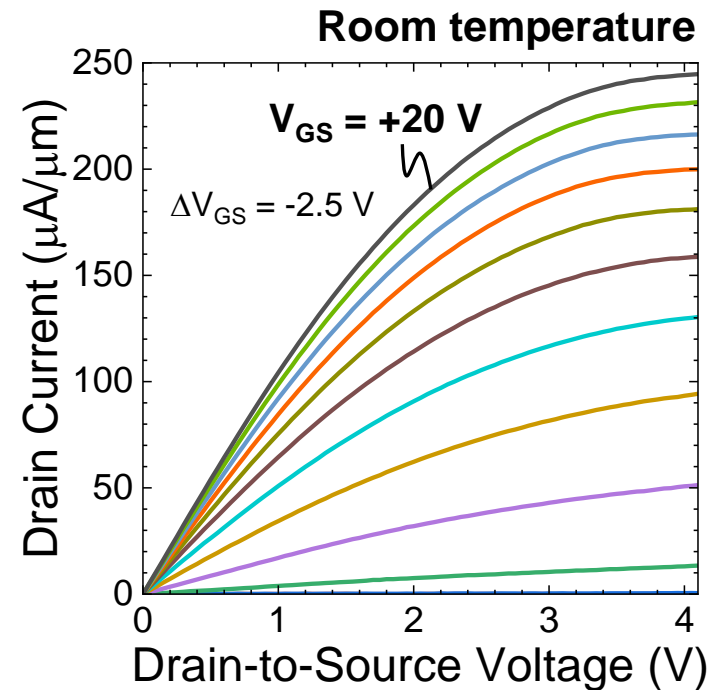
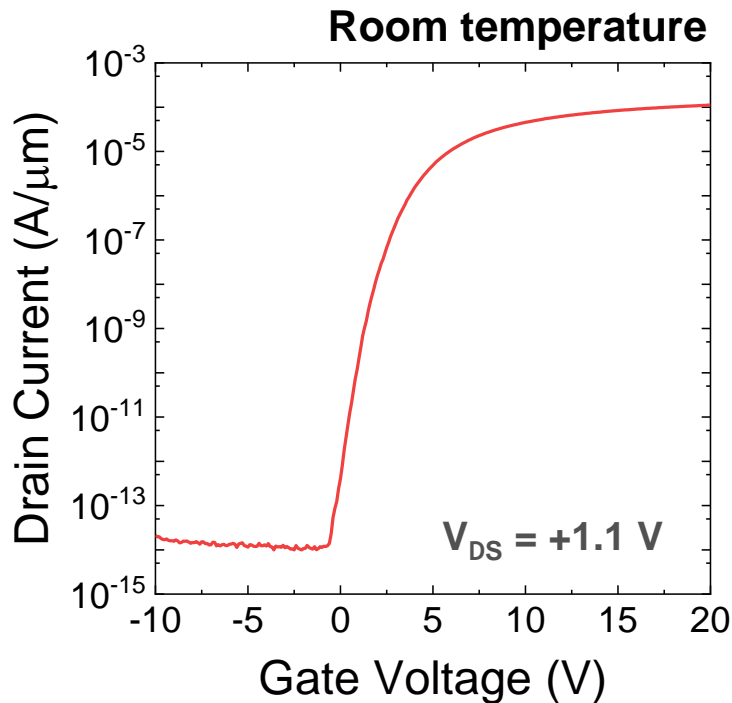
- Devices used a dual-gate geometry to better study contacts.**

Work funded by Intel.

# *WS<sub>2</sub> MOSFETs with Bi Contacts*

- Dual-gated results for devices with  $L_{\text{EFF}} = 0.32 \mu\text{m}$ :

L. Jin and S. J. Koester, IEEE EDL 43, 639-642 (2022).

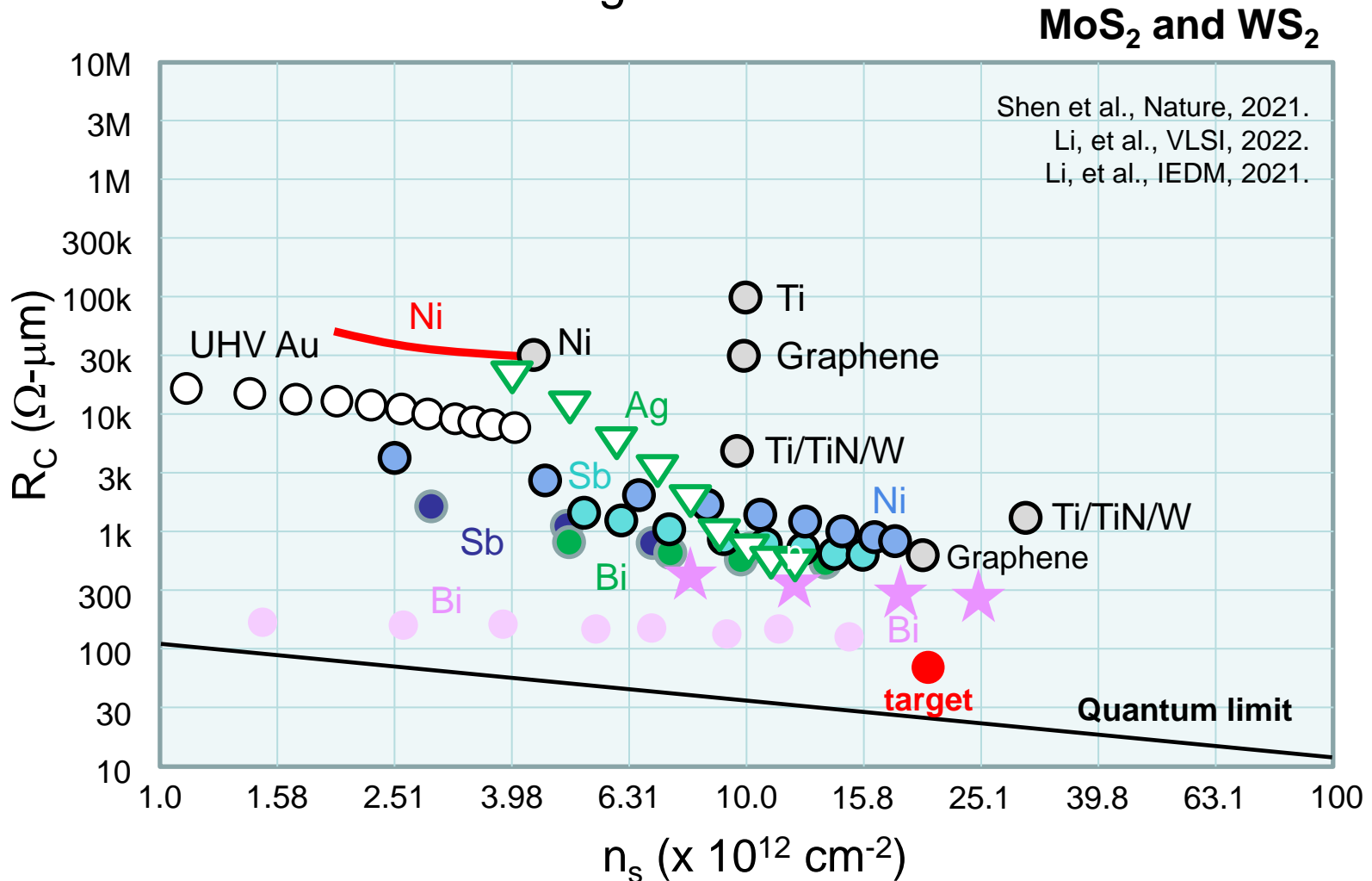


- Devices have large ( $10^{10}$ ) ON/OFF ratio and high drive current of  $245 \mu\text{A}/\mu\text{m}$  (for relatively long gate length).**

Work funded by Intel.

# 2D Contact Resistance Progress

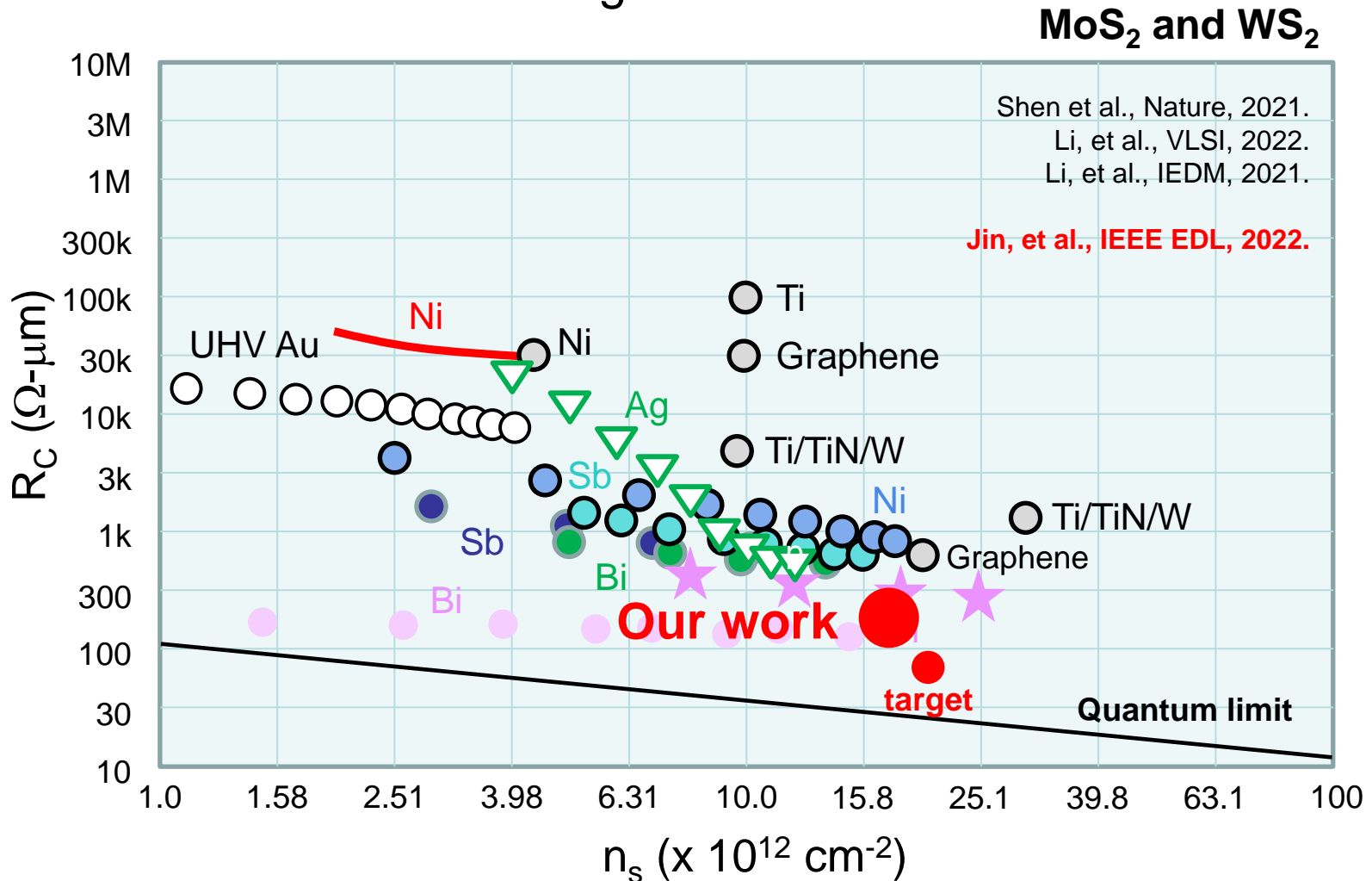
- Semi-metallic contacts have greatly improved prospects for TMDCs to meet IRDS targets:





# 2D Contact Resistance Progress

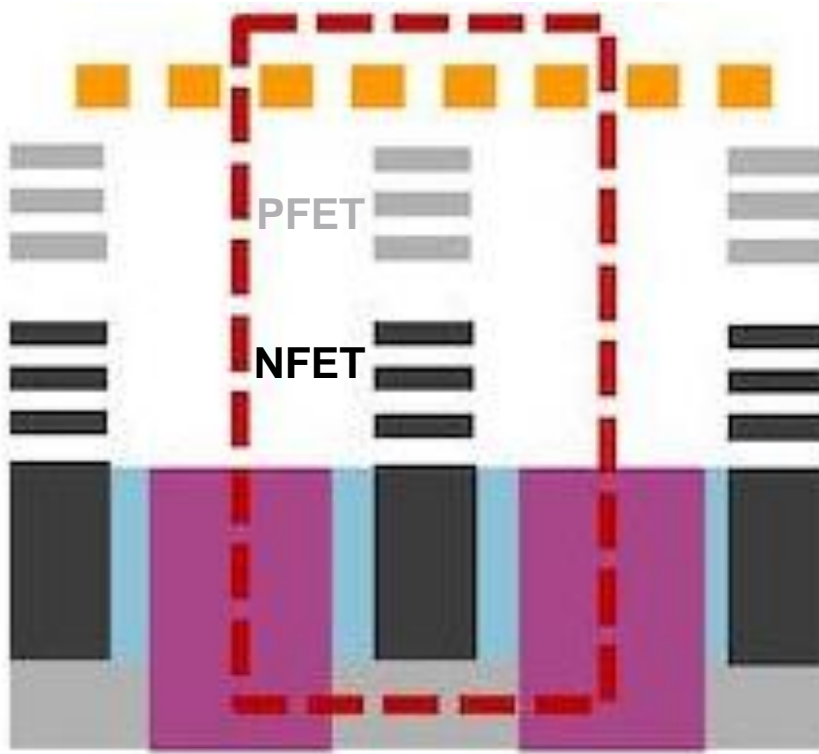
- Semi-metallic contacts have greatly improved prospects for TMDs to meet IRDS targets:



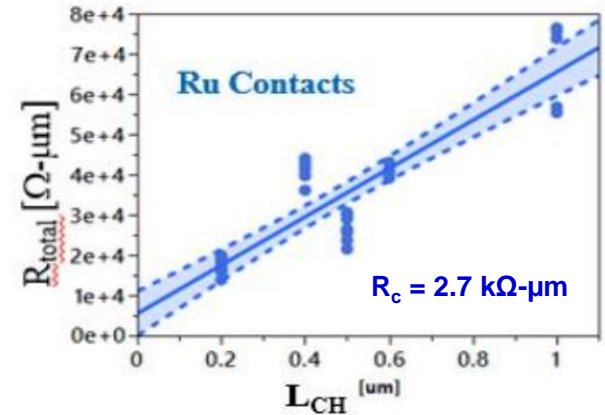
# Future Logic Outlook

- Ultimate goal is stacked nanosheet CMOS.
- Recent work has started to address outstanding challenges for PFETs and 3D device structures.

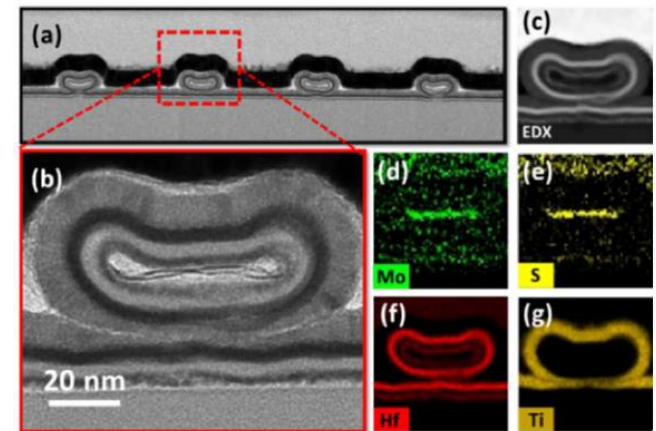
Source: imec



K. O'Brien, et al., IEDM, 2021.  
Chiang et al., EDL, 2022.



Y.-Y. Chung, et al., IEDM, 2022.

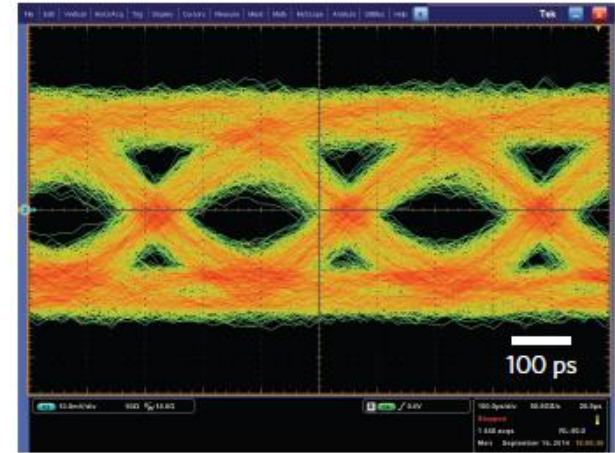
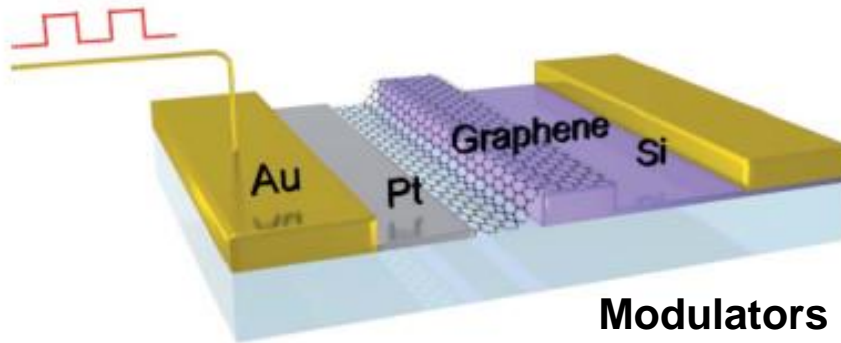


# 2D Integrated Optoelectronics

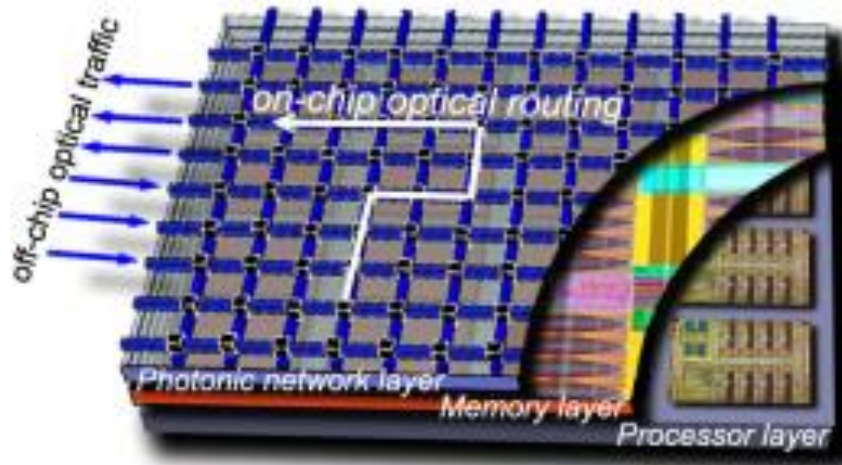
- 2D materials have a wide range of optoelectronic applications:

M. Liu, et al., Nature, 2021.

N. Youngblood...S. J. Koester, et al., Nat. Photon. 9, 247, 2015.



Source: IBM

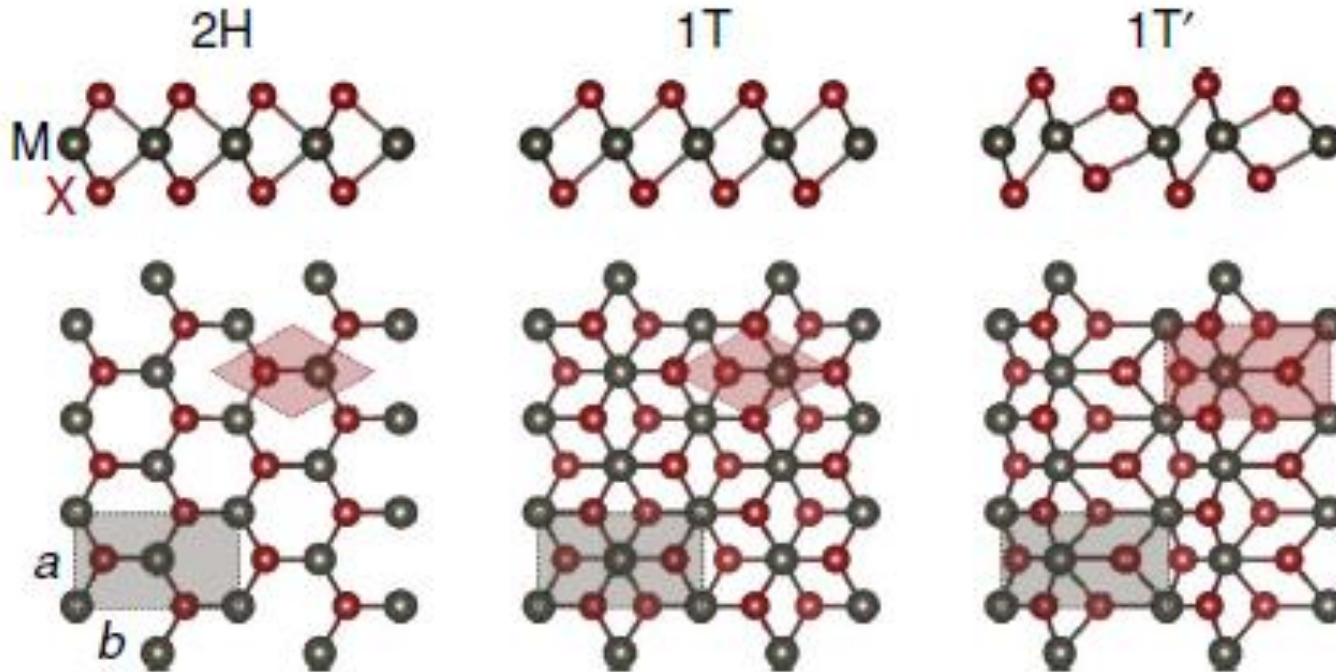


- Could be used BEOL-compatible optical interconnects with high speed and large spectral bandwidth.

# Phase Engineering in 2D Materials

- TMDCs have the interesting property that can exist in either a semiconducting or metallic phase:

Y. Li, et al., Nat. Commun., 2015.



Hexagonal (2H)  
Semiconducting

Tetragonal (1T)  
Metallic

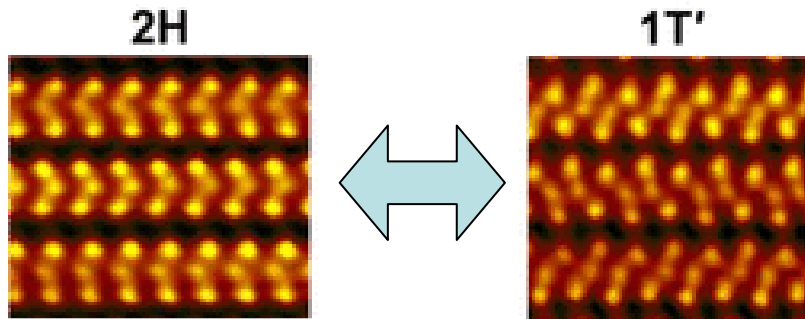
Monoclinic (1T')  
Semi-metallic



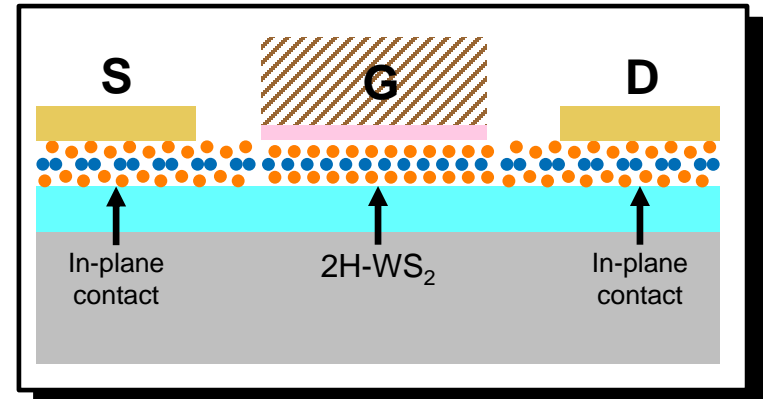
# Phase Engineering in 2D Materials

- Ability to control TMDC phase could open the door to a multitude of applications:

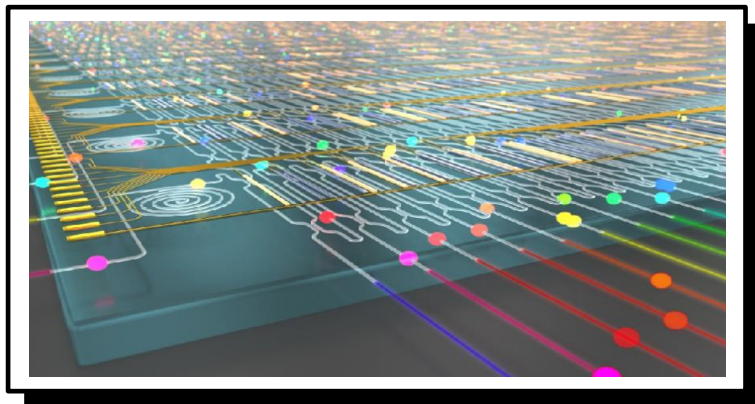
R. Ma...S. J. Koester, et al., ACS Nano 13, 8035-8046 (2019).



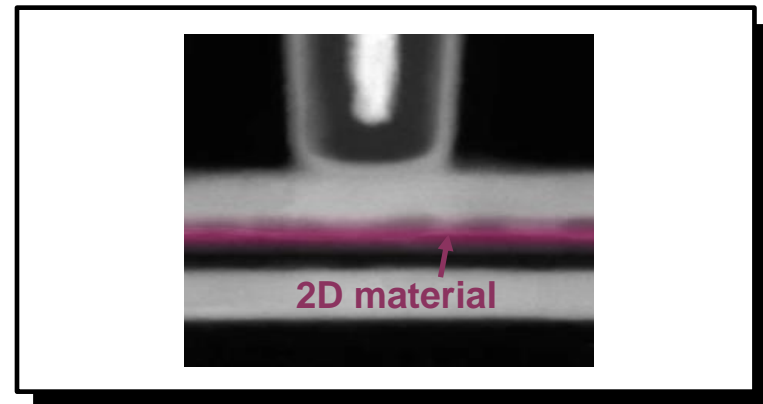
## High-performance MOSFETs



## Reconfigurable optics



## Memristors



# Conclusions / Interactions

- 2D semiconductors have significant potential 3D / embedded memories and sub-1-nm-node CMOS applications.
  - 2D materials also have potential for many emerging applications such as integrated optoelectronics and memristors.
- 
- US / Korea research interactions could help to enhance technology development in 2D materials. Current interactions:
    - UNIST – Collaboration on novel 2D optoelectronic devices.
    - Organized Quantum Phenomena winter school at UMN in 2023, with support from Kyunghee University, Korean Science Foundation and NSF Global Quantum Leap program.
    - President Joan Gabel of the UMN signed with Hanyang University and KIST, working to expand these interactions Seoul National University as well.



***Thank you for your attention!***