Abstract

This paper presents a method for feature detection and matching on Field Programmable Gate Array (FPGA) for long-range, stereo vision applications where speed matters. Computer vision algorithms have been extremely data-intensive, requiring power-hungry, multi-core, high-clockspeed CPUs in order to do computations in real-time. The alternative is to architect algorithms for parallel implementation on FPGA. The work presented in this paper uses a new metric to compare the throughput, energy, and time required to compute a solution for a given processor: GB/(J*s). Using this metric, the FPGA was able to compute XXX GB/(J*s) while the state-of-art CPU took XX GB/(J*s). The result is an XX improvement of FPGA over CPU implementation.