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Impact of Scaling on Thermal Behavior of Silicon-on-Insulator Transistors

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ABSTRACT

In this manuscript, the impact of scaling on self-heating of silicon-on-insulator (SOI) transistors is investigated. For the first time the effect of temperature dependent phonon-boundary scattering in silicon thin films, which results in reduction in thermal conduction in the channel region, is incorporated to the hydrodynamic simulation of electrons and holes in a commercial electro-thermal simulation tool. Results of DC electro-thermal simulations are used to study drain current degradation due to self-heating and to obtain the thermal resistance of SOI devices as a function of the gate length and silicon layer thickness. The device thermal resistance is increased by more than a factor of 2 due to the scaling of gate length from 180nm to 45nm. Neglecting phonon-boundary scattering in the channel region may underestimate the degradation of drain current due to self-heating by nearly a factor of two. Thermal resistance of SOI devices with 25nm silicon layer can be up to 8 times larger than that of bulk devices.

NOMENCLATURE

C= capacitance (F)
d= thickness (m)
f= switching frequency (Hz)
I= current (A)
k= thermal conductivity (W/m-K)
L= device length (m)
P= power (W)
$R_{thermal}$= device thermal resistance (K/W)
T= temperature (K)
V= voltage (V)
W= device width

Subscripts:

avg = average
d= drain
g= gate
max= maximum

off= off state for a transistor
Si= silicon
s= source
sat= saturation region for a transistor
t= threshold

INTRODUCTION

Silicon-on-insulator (SOI) devices exhibit an enhanced performance compared to bulk CMOS (complementary-metal-oxide-semiconductor) transistors [1]. Owing to reduced junction capacitance, gate delay in an SOI logic component can be improved by nearly 25% [2]. Especially, when the fan out of a logic gate is small (e.g., one), improvement in the gate delay over bulk MOS is considerable [3]. More than 20% increase in the clock frequency of a 64-bit CPU (central processing unit) using 0.2μm SOI technology has been reported [4]. Depending on the supply voltage, total power consumption (including both static and dynamic power dissipations) of an SOI inverter can be as small as half of the power consumed by a CMOS inverter with the same feature sizes [5].

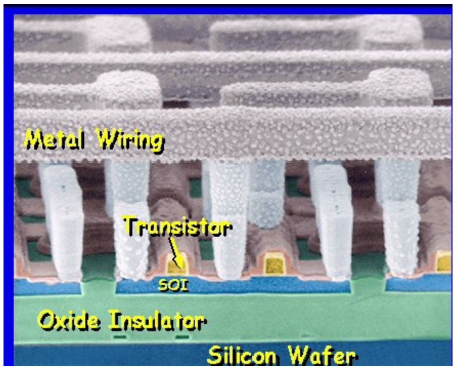


Fig. 1 Structure of an SOI transistor (IBM, 2000).

Fig. 1 shows the cross-section of an SOI transistor. Because of the buried silicon dioxide layer (BOX), SOI devices have, good radiation hardness, no latch up, and enhanced capability in high device density [6]. The dielectric constant, ε, of silicon dioxide (~3.9) is more than three times smaller than that of silicon (~11.9). Therefore, SOI devices show parasitic junction capacitances, which are much smaller than those of bulk transistors [7]. It is well-known that dynamic power consumption of a logic gate is equal to $(1/2)CV^2f$ where C is the total capacitance at the output node of the logic gate, V is the supply voltage, and f is the switching frequency [8]. Due to small capacitance offered by SOI technology, for a given clock frequency and supply voltage, the dynamic power consumption of SOI devices is small. Compared to bulk MOS devices, power dissipation and speed performance in SOI transistors are less sensitive to scale down of the power supply, therefore SOI technology is more practical for low power circuits [1]. Off leakage current in SOI devices can be three orders of magnitude less than that of bulk transistors at room temperature [9] and the threshold voltage has week dependency on the substrate voltage [10], which results in a reliable performance.

Two types of SOI devices are widely used: partially depleted (PD) [11] and fully depleted (FD) [12]. Thickness of the silicon layer in a PD transistor is typically larger than 100nm, subsequently the active layer is not fully depleted. For an FD transistor, thickness of the silicon film is less than 100nm, therefore, during the normal operation the silicon layer is fully depleted. Comparing these two types of SOI devices, FD exhibits advantages in kink effects and history dependence and PD shows improvements in short channel effects, manufacturability, and offering multiple threshold voltages [13].

In spite of the enhanced performance of SOI devices offered by BOX layer, due to the low thermal conductivity of silicon dioxide (~1.4 W/m-K at room temperature), this layer severely impedes heat conduction to the substrate. Therefore, compared to bulk MOS devices, SOI transistors are potentially more prone to self-heating [14]. An additional phenomenon which significantly contributes to the self-heating is phonon-boundary scattering at the boundaries of the channel region [15]. This effect cannot be explained by continuum assumption and as the result; thermal sub-continuum theory has to be included in investigating self-heating and reliability of SOI devices. In our previous work, we investigated some of major thermal sub-continuum effects including phonon-boundary scattering in thin films through experimental measurements and numerical treatment of BTE for phonons [16-23]. Recently we have been able to incorporate some of these effects into a commercial electro-thermal simulator, TCAD, to account for number of nanoscale thermal phenomena and some results have been reported in [18,24].

The goal of this manuscript is to quantitatively study the effect of scaling on self-heating in different generations of SOI devices. In the present work, for the first time, we incorporate the temperature dependent phonon-boundary scattering to hydrodynamic simulation of electrons and holes in order to account for the impact of nonlocal transport of electrons, holes, and phonons on electrical and thermal performance of SOI transistors. In the following section, the impact of self-heating on the performance of and reliability SOI is discussed. Next section is dedicated to modeling of phonon boundary scattering in thin silicon films above room temperature. That will be followed by describing the hydrodynamic (HD) model and its relevance to the simulation of sub-0.2μm SOI devices. Subsequent part explains the implementation of different generations of SOI technology in the commercial electro-thermal simulator, TCAD. Finally, the results of electro-thermal simulations, which account for phonon-boundary scattering, are reported. The dependency of device thermal resistance on gate length and silicon thickness is discussed.

SELF-HEATING, AND RELIABILITY OF SOI DEVICES

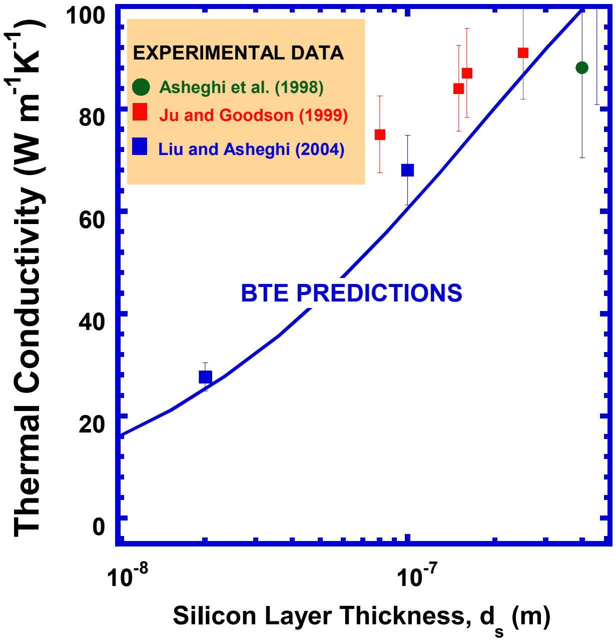
Self-heating: Under steady state (DC) operation, saturation current, I_{sat}, of an SOI device can be smaller than that of bulk device. One reason is that as temperature increases, more electron-phonon scattering occurs which in turn reduces the mean free path of electrons and results in reduced mobility. Mistry, et. al, reports that for 100nm gate length devices, I_{sat} of an SOI device is 9% smaller than saturation current of a bulk CMOS transistor [3]. Self-heating has been considered to be responsible for 6-7% of this reduction and the other 2-3% comes from larger threshold voltage (by 40-50mV) for the SOI device. Degradation of I_{sat} adversely affects the figure of merit (FOM) of SOI technology that is defined as I_{sat}/I_{off} [25]. I_{off} is the leakage current when a transistor is off. This leakage current exponentially increases as lattice temperature elevates and as the result, self-heating suppresses FOM by attacking both I_{sat} and I_{off} [26]. Moreover, increase in the leakage current results in additional power consumption and is not affordable for portable devices, which rely on a battery for their operation.

As explained earlier, increased temperature can result in reduced mobility. At relatively high drain voltage, this effect is translated to a so-called negative differential output resistance [27]. It turns out that for SOI devices operating at a low temperature (e.g., 77K) the behavior of negative differential output impedance is more pronounced indicating that self-heating for SOI devices is more severe at lower temperatures [28]. Large sensitivity of electron mobility to the temperature and small thermal conductivity of silicon and silicon dioxide at low temperatures are main reasons for this increased self-heating. Predictions indicate that thermal resistance of an SOI device with L_g= and d_{Si}= at 40K is ~ 6 K/mW and is 2.7 times larger than the value at room temperature [21].

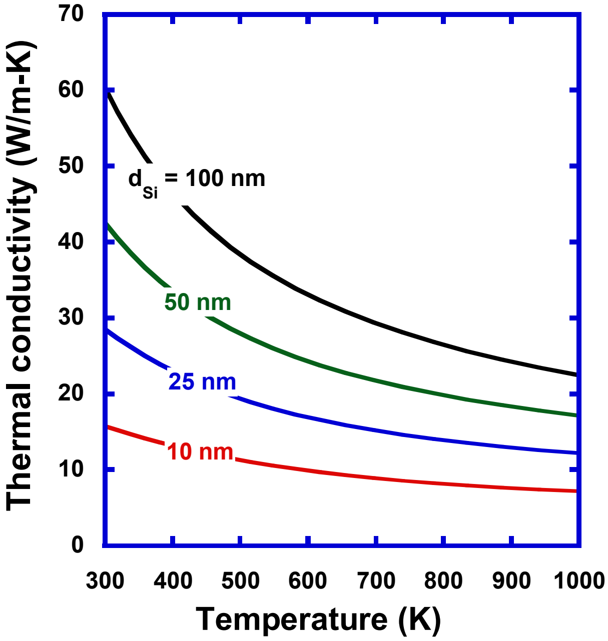
Depending on the application, self-heating may or may not impose a serious impact on the operation of SOI circuits. The self-heating effect on digital elements is small [13]. In digital circuits, the power is mostly consumed during the transition between high and low states. The power consumption and lattice temperature in a nearly FD (NFD) SOI NMOS switch with a channel length of 0.2μm were reported to be ~0.13 mW and 0.7K respectively [29]. Another publication indicates that the temperature of a PD NMOS transistor with a gate length of 0.7μm during switching does not exceed 2.5K [30]. Additional reason for this minimal temperature rise in digital components originates from the small heat penetration depth associated with short time-scale switching in these devices. As explained in [19], the heat penetration depth is proportional to the square root of the heating time-scale and determines the device dynamic (transient) thermal resistance. Subsequently, due to the small time-scale of switching process, dynamic thermal resistance of digital elements is relatively small. The conclusion is that the impact of self-heating on devices which work only as digital components and are not thermally coupled to the rest of the circuit, can be negligible. However, self-heating can significantly degrade the operation of analog circuits. It has been shown that because of the self-heating, gain of a class-A amplifier made of PD SOI NMOS transistors with a channel length of 0.7μm can be reduced by more than 0.1dB [30]. The same work reports that non-linear temperature change in a 7-bit DAC (digital to analog converter) implemented in

0.7μm PD SOI technology, makes the step size of the DAC's output voltage to be nonlinear and degrades the overall performance [30].

Device structure and dimensions determine the capability of an SOI transistor on dissipating heat. In particular, drain-to-gate separation, gate length, channel thickness, and layout of the structure have significant impact on thermal resistance and temperature rise of SOI devices [31].



(a)



(b)

Fig. 2 (a) Measured data for effective lateral thermal conductivity of silicon thin films and nano-wires as a function of the film thickness and wire diameter at room temperature; (b) predictions for thermal conductivity of silicon thin films for different film thickness based on the model by [39].

In some circuits such as current mirrors, *thermal coupling* between adjacent SOI devices can affect the performance of the circuit. If the layout of the two transistors making a current mirror is in such a way that both devices share the source region, heat generated in the output transistor can propagate to the input device and reduce the current [32].

Reliability: Electrostatic discharge (ESD) and electrical overstress (EOS) are two major reliability issues, which are directly related to thermal behavior of a device. For time to failure of 10nSec, power to failure of a 0.4μm NMOS SOI is around 0.5W and is 3 times smaller than that of a bulk transistor which indicates that SOI devices are more susceptible to ESD failures [33]. For positive Human Body Model (HBM) stresses, ESD failure voltage of SOI devices with channel lengths from 0.5μm to 1.5μm are about 500V and are almost half of the failure voltage for bulk transistors [34]. Modeling of ESD is out of scope of this letter and the authors will focus on this issue in future.

PHONON TRANSPORT IN SILICON THIN FILMS

Phonons, which are quanta of lattice vibration, are dominant heat carriers in semiconductors and dielectrics over a wide temperature range [35]. As shown in Fig. 2(a), experimental data indicate that thermal conductivity of thin silicon layers can be much smaller than that of bulk material [21-23]. In most of SOI devices, the thickness of silicon layer is below 200nm and the reduction in thermal conductivity has to be accounted for. Recent results indicate that lateral thermal conductivity of 20nm silicon layer with crystal orientation of <110> at room temperature is ~25 W/m-K whereas thermal conductivity of bulk silicon which is 148 W/m-K [21]. This reduction in thermal conductivity is due to phonon-boundary scattering and cannot be explained by continuum theory, as the result sub-continuum theory needed to be involved [36].

Surface roughness has direct impacts on the quality of phonon-boundary scattering such that for rough surfaces (relative to phonons wavelength), scattering at boundaries can be fully diffuse [37]. Under this condition, scattered phonons at the interface lose their memory in the sense that it is not possible to determine whether a phonon leaving the interface is due to the transmission from the other side or reflection from the same side. Asheghi et. al, [23] report that for the case of silicon thin layers on oxide, interface roughness is ~10Å and this value can explain the experimental data for thermal conductivity obtained in that work. Following the models presented by Beckmann and Spizzichino [38], Asheghi et. al [23] concludes that phonon scattering at the interface between silicon and silicon-dioxide is fully diffuse.

To capture temperature dependent phonon-boundary scattering, Liu et. al [39] proposes an analytical model, which can predict the lateral thermal conductivity of pure and doped silicon thin films at high temperatures (300K and above). The agreement between this model and experimental results are good. This approach is based on a model originally presented by Holland [40] which accounts for individual contribution of transverse and longitudinal acoustic phonons. The new model by Liu et. al [39] incorporates a reduction factor for mean free path of different branches to account for phonon-boundary scattering in thin films. Using this analytical model, thermal conductivity of 10nm, 25nm, 50nm, and 100nm silicon thin films at high temperatures is obtained (see Fig. 2(b)). This data is incorporated to TCAD to perform simulations on SOI devices.

HYDRODYNAMIC SIMULATION OF ELECTRONS AND HOLES

As the device feature size shrinks down below 200nm, velocity overshoot that is a nonlocal transport effect associated with electrons and holes prevails. Conventional drift-diffusion model fails to capture this effect and subsequently underestimates the drain current of SOI transistors by as much as 25% [41]. The drift-diffusion model also overestimates the impact ionization rates in deep-submicron regime. However, both experimental data and the Monte-Carlo (MC) simulation to the Boltzmann Transport Equations for charge transport are capable of exhibiting the velocity overshoot [42,43]. Although the Monte-Carlo is the most rigorous approach to study charge transport, it is a computationally expensive method. The hydrodynamic model [44] is a moments of the BTE and can explain the velocity overshoot. However, its implementation is not as time-consuming as the MC and therefore it is considered as a practical alternative to the MC. The details of the HD model used in the present work can be found in [45]

SCALING OF SOI TRANSISTORS

Coupled electro-thermal simulations in TCAD are performed to study the effect of scaling on self-heating and performance of SOI transistors. While number of short channel effects are considered in these simulations, due to high complexity level of the problem, several phenomena such as effect of interconnects, nonequilibrium electron-phonon scattering, and quantum effects have not been included in this work. We should emphasize that although the results presented in this work can capture the trend for thermal behavior of different generations of SOI devices, the uncertainty of many parameters involved in the simulation of these transistors affect the accuracy of the presented data.

Physical gate lengths, L_g, correspond to different generations are obtained from International Technology Road Map of Semiconductors (ITRS) [46]. For each technology node, five devices, one representing bulk MOS transistor and four SOI structures with silicon thickness (d_{Si}) of 10nm, 25nm, 50nm, and 100nm are constructed in the simulator. Gate oxide and BOX are 3nm and 450nm thick, respectively and spacing between drain/source contacts and gate are chosen to be L_g. Width of devices are assumed to be $3\times L_g$. Drain and source are doped with Arsenic and have Gaussian doping profiles with peak value of 6×10^{20} cm^{-3}. Substrate is lightly doped with Boron and doping concentration is 3×10^{17} cm^{-3}. Figure 3 shows the doping profile in an SOI device with L_g = 45 nm and d_{Si} = 25 nm. Recent experimental data shows that thermal conductivity of a 30nm silicon thin film doped with Arsenic with concentration of 2.3×10^{20} cm^{-3} is ~15 W/m-K at room temperature [47]. This value is almost half of the thermal conductivity of a 30nm nearly pure silicon thin film and the reduction is due phonon-impurity scattering. After examining the doping profile and thermal boundary conditions applied to drain/source contacts, it is concluded that neglecting phonon-impurity scattering results in negligible error in our final results. Substrate, drain, and source contacts are kept at 300K. Gate contact is considered to be adiabatic and convection and radiation are neglected. Size of the simulation domain is chosen to be large enough such that boundaries do not interfere with electrical and thermal activities in the channel.

In all the simulations, V_{gs} is 1V and drain voltage is swept from 0V to 2 V to extract several quantities including I-V curve, threshold voltage, and temperature profile. For all the simulations, source and substrate are at 0V. For each device, three simulations are performed: 1) *no-self-heating*: lattice temperature is assumed to be always at 300K. It is equivalent of pulsed-measurement where in the actual experiment, pulses applied to a device are chosen to be short enough such that the I-V curve of a transistor can be sampled without elevating the lattice temperature [8]; 2) *continuum*: simulations based on thermal conductivity of bulk silicon; and 3) *sub-continuum*: simulations using the reduced temperature dependent thermal conductivity which accounts for phonon-boundary scattering as depicted in Fig. 2(b). In the next section we report the results of the *sub-continuum* simulations.

RESULTS AND DISCUSSION

As discussed earlier, device ability in providing and maintaining a desired level of drain current has direct impact on figure of merit and performance of electronic circuits. One of the main concerns associated with performance of SOI transistors is current degradation due to self-heating and understanding this behavior is valuable. The generated power in the device for a given bias condition as well as the ability of

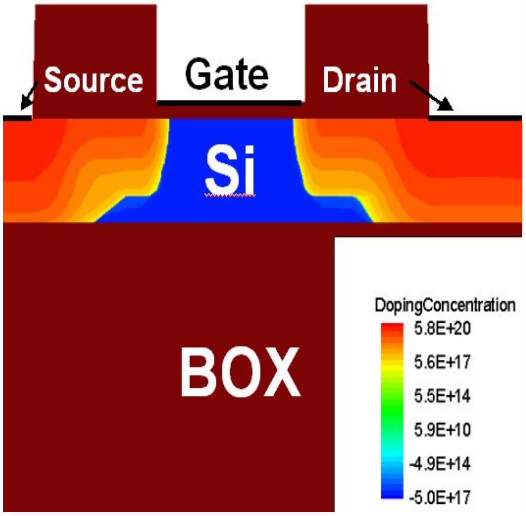


Fig. 3. Doping profile in an SOI transistor with gate length of 45nm and silicon thickness of 25nm.

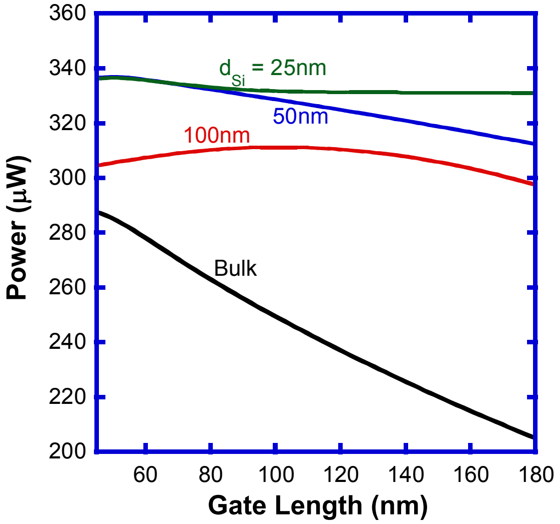


Fig. 4. Power as a function of the gate length and silicon thickness (V_{gs}=1V and V_{ds}=2V).

dissipating such power are two main factors tied to the self-heating. Both these key factors are studied in the following section.

Results of the sub-continuum simulations are used to calculate the static power $P=V_{ds}\times I_{ds}$ for each device at V_{ds}=2 V and V_{gs}=1 V. As shown in Fig. 4, for a given V_{ds} and V_{gs}, generated power increases as the devices become shorter. Due to short channel effects, threshold voltage increases as channel length decreases and subsequently drain current decreases [48]. Also velocity overshoot is more pronounced for shorter gate lengths, which further increases the drain current [41]. Furthermore, for thinner silicon layers gate has more control on the channel and therefore the threshold voltage decreases as the thickness of the silicon increases. This explains the thickness dependency of the static power as presented in Fig. 4. On the other hand, as we will see later self-heating is more severe in smaller devices with thin silicon layers which decreases the mobility and the drain current and partially suppresses the enhanced impact of the reduced threshold voltage and velocity overshoot. This can be inferred by different slopes correspond

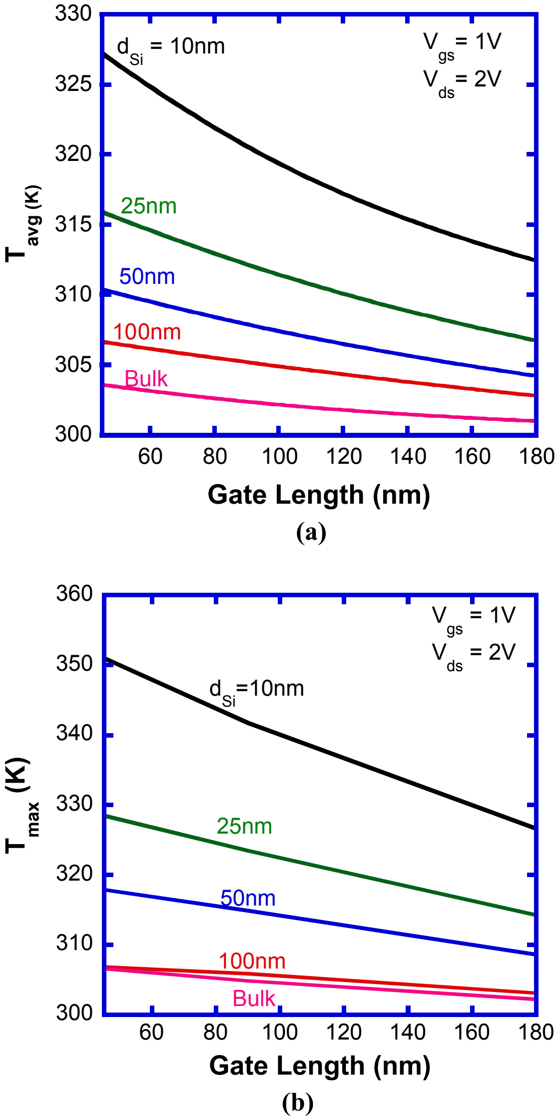


Fig. 5 (a) Average and (b) maximum temperature of the device as a function of gate length and silicon thickness.

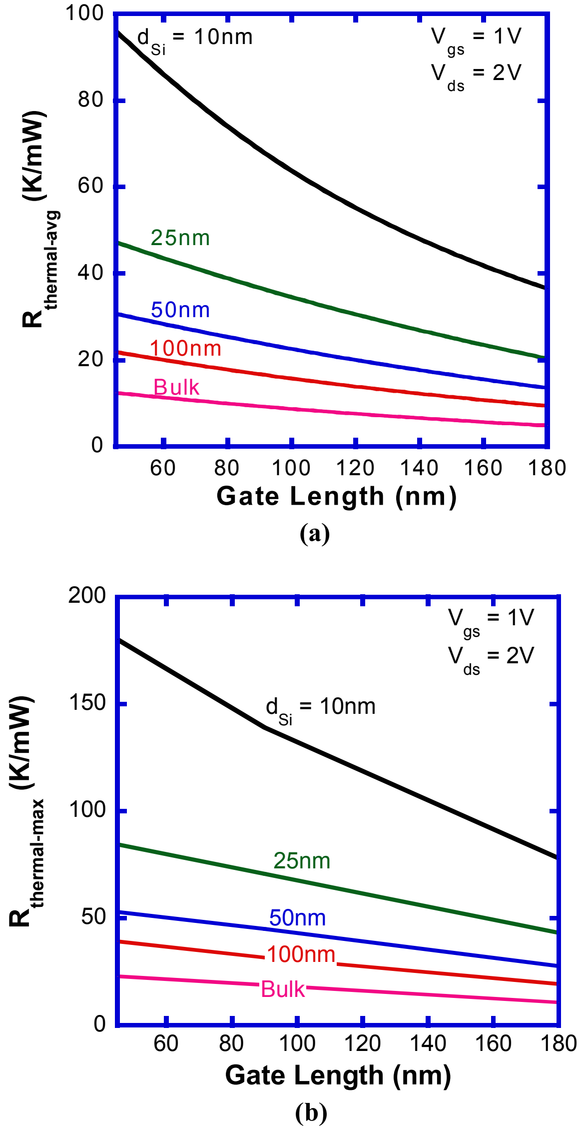


Fig. 6 (a) Average and (b) maximum thermal resistance as a function of gate length and silicon thickness.

to different curves on Fig. 4. Comparing the results of the hydrodynamic simulations presented in this work with the results of drift-diffusion model [24], one concludes that due to the absence of velocity overshoot in the drift-diffusion model, the latter underestimates the drain current and the static power and as the result it can not correctly capture the trend for the static power as a function of the gate length. One should note that the thermal boundary conditions applied in [24] is more aggressive than the ones imposed in the present work, which significantly reduces the estimated drain current for a given biasing condition.

T_{avg} and T_{max} are defined as the average temperature along the channel and maximum temperature at the hotspot, respectively. The average temperature along the channel is particularly of interest when the degradation of mobility and threshold voltage due to self-heating is studied. Maximum temperature is an important parameter when reliability of transistors is investigated. Figure 5(a,b) summarize simulations results for T_{avg} and T_{max} as functions silicon layer thickness and gate length. Based on concepts of average channel temperature and maximum junction temperature, average thermal resistance, $R_{thermal-avg} = (T_{avg}-300) / P$, and maximum thermal resistance, $R_{thermal-max} = (T_{max}-300) / P$, are determined (see Fig. 6). There are several facts which explain the behavior of thermal resistances shown in Fig. 6: 1) larger devices offer more area for heat dissipation, therefore, their thermal resistances are relatively small which result in small temperature rise; 2) thermal resistance of devices with thicker silicon layer is small because: i) the volume of heat dissipation in the channel is larger, and ii) effect of phonon-boundary scattering on thermal conductivity is less pronounced (Fig. 2(a)). This argument is consistent with the analytical model for thermal resistance of SOI transistors proposed by [49] which suggests that thermal resistance of SOI devices is proportional to $d_{Si}^{-0.5} \cdot k_{Si}^{-0.5}$. It is worth nothing that the difference between R_{th-avg} and R_{th-max} for a bulk device or for an SOI transistor with thick silicon layer is not large, whereas, this difference for an SOI device with 45nm silicon layer can be more than 80% suggesting a relatively large temperature gradient along the channel. This is consistent with the temperature profile extracted from the simulations results.

CONCLUSION

Importance of thermal sub-continuum effects in modeling of self-heating in SOI devices was explained. Impact of temperature dependent phonon-boundary scattering on thermal conductivity of silicon thin films was included in hydrodynamic simulation of SOI transistors. It was explained that the drift-diffusion model can not capture the velocity overshoot which is a nonlocal effect and therefore underestimates the drain current, static power, and self-heating in the device. Dependency of thermal resistance of SOI devices on gate length and silicon layer thickness was investigated. Several issue such as the effect of silicide, interconnects thermal resistance, non-equilibrium electron-phonon scattering have to be included in the simulations to achieve higher accuracy.

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