

"CMOS Scaling for The Next Decade: Status, Challenges and Opportunities"

Prashant Majhi

Abstract:

CMOS scaling has, and will continue to, provide the means to realize higher performance with every technology node. The advent of high-k/metal gates into production for current and future generation CMOS gate stacks has marked the onset of MOSFET scaling that has clearly become reliant on new materials and / or new device architecture. Also, recently, there have been very promising results on controlling junctions and contacts for short channel devices. More specifically, new approaches to form ultra-shallow junctions with high active-dopant concentrations and low schottky barrier height silicides with novel materials to reduce contact resistance have been reported by many groups. These advances (that are additive to process-induced strain) may be transferred onto non-planar devices as well, ensuring CMOS scaling for more generations to come. While we continue to address the remaining challenges of scaled devices (both planar and non-planar), it is becoming clear that Si (as the channel) may not be able to provide for the high performance combined with low power technologies that would be needed in future. Over several years, there has been a lot of research on high mobility channels: group IV for pMOSFETs and III-V for NMOSFETs. However, there appears to be little consensus on a) the choice of high mobility channels for P and N channel MOSFETs, b) its potential compared to short channel strained-Si, and 3) potential technology node for insertion. In this tutorial, trends, challenges and opportunities related to several of the aforementioned modules will be presented and discussed.