Fabrication and Characterization of bulk FinFETs for Future Nano-Scale CMOS Technology

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ABSTRACT

Starting with brief explanation of SOI double/triple-gate MOSFETs ever reported, device structure of body-tied double/triple-gate MOSFETs is introduced. The body-tied double/triple-gate devices were invented by our group, and have been implemented on bulk Si wafers instead of SOI wafers. We call them as bulk FinFET sometimes because the fin body was directly connected to the Si substrate. The bulk FinFETs have advantages such as lower wafer price, lower defect density, much less back-bias effect, similar device scalability, much less heat accumulation over SOI FinFETs. Using 3-dimensional device simulator, we studied the devices extensively. We will show key features and simple design guideline of the device from the results of 3-dimensinal device simulation. The body-tied double/triple-gate MOSFETs were fabricated and the characteristics were compared with those of conventional planar channel devices. Detailed fabrication process steps are explained. We applied this device technology to SRAM cell and achieved operational six-transistor SRAM cell. A cell size of 0.90 um^2 was achieved in 90 nm node technology, with stable operation at 1.2 V using 4 levels of W and Al interconnects. Static noise margin of 280 mV was obtained at V_{CC} of 1.2 V. The device structure of the double/triple-gate MOSFETs was applied to flash memory technology and show you some results. The bulk FinFETs has nearly the same process compatibility to conventional planar channel MOSFETs technology and can be applied to logic ICs, SRAM, DRAM, flash memory, and so on.