Additive Manufacturing of Micro and Nanoscale Electronics for Heterogenous Integration and Advanced Packaging;

a Semiconductor Foundry in a Box

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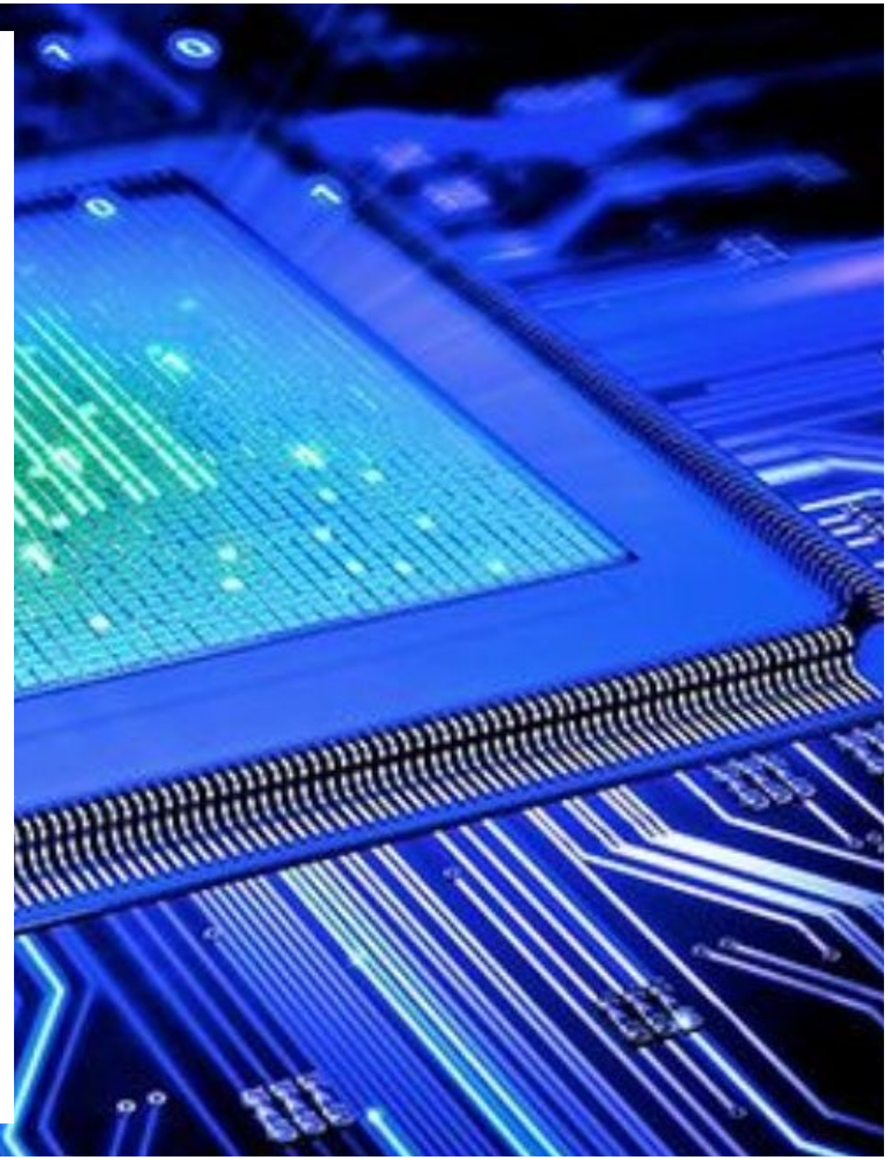
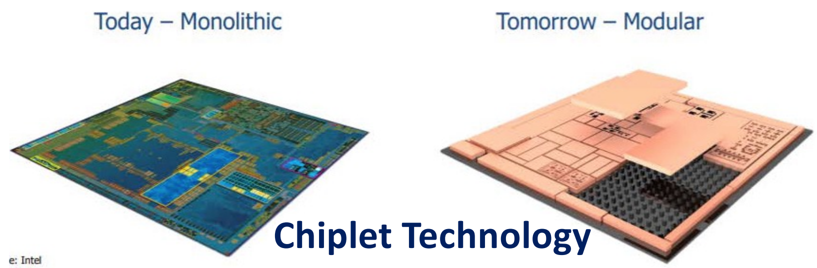
- Introduction
- Additive manufacturing Using Directed Assembly-based Processes
    - Electrophoretic Assembly (EPx Platform)
    - Fast fluidic Assembly (FFx Platforms)
- Manufacturing of crystalline and single-crystal of metals and semiconductors
- Applications (Adv. Packaging, capacitors, transistors, logic gates, etc.)
- Scalable and fully automated Fab-in-a-Box
- Summary

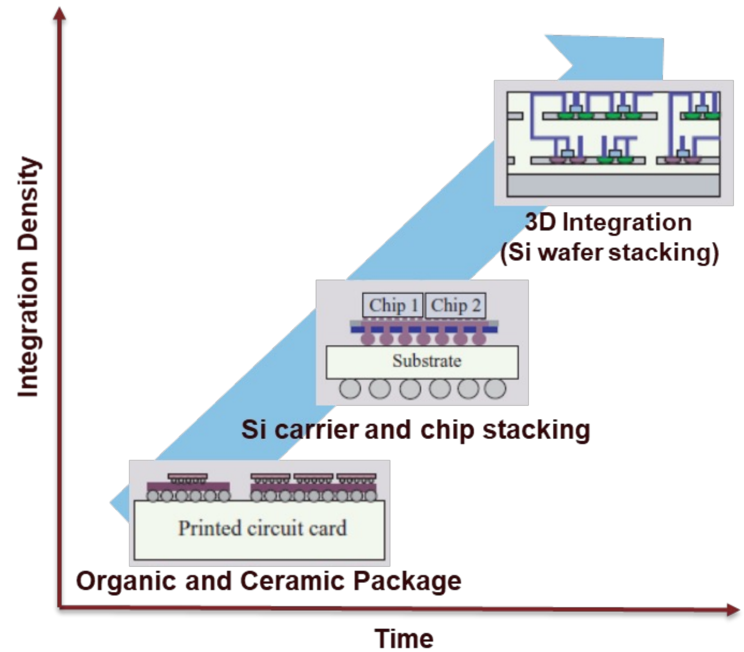


Fine Resolution Interconnects, Passive and Active Components for Advanced Packaging



Currently, 3D heterogeneous integration utilizing fine resolution (< 2 microns) trace, passive and active components on interposers are made using conventional fabrication in foundries. This introduces many challenges, among them:

- Long lead times (> 12 months) and High costs
- No on-demand capability limiting innovation.
- Limits of the type of materials for heterogeneous integration in manufacturing
- Thermal management and trojan sensors can be made at the same time.



Additive manufacturing will enable lower costs, a faster development cycle, smaller boards, faster and more reliable packages, and more material choices.

What if?

You can make your chip or advanced package

- **in one day**
- **on one fully automated machine**
- **at 100 times less cost**
- **25 times smaller carbon footprint**

Yes!

The New Future of Electronics Manufacturing is Here

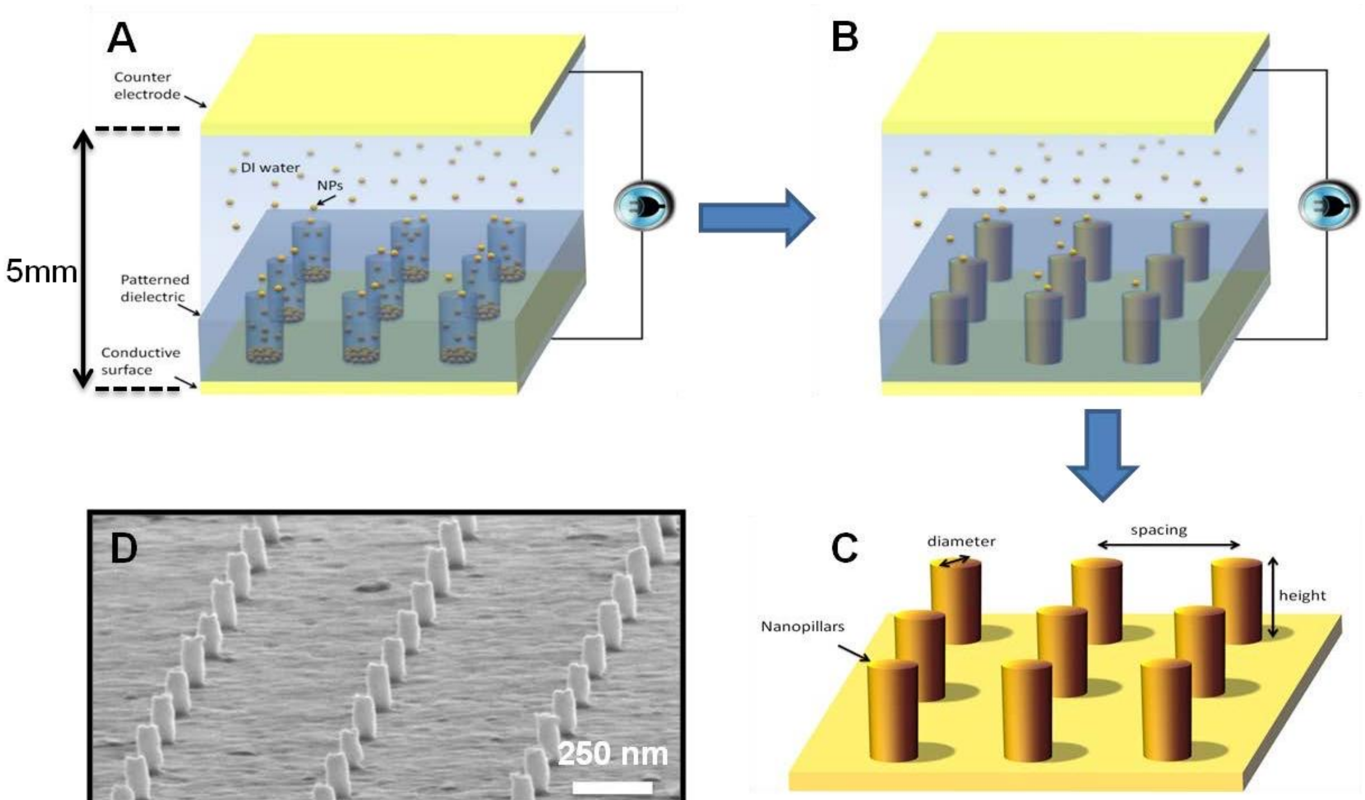
Additively manufactured electronics made using any material on any surface.

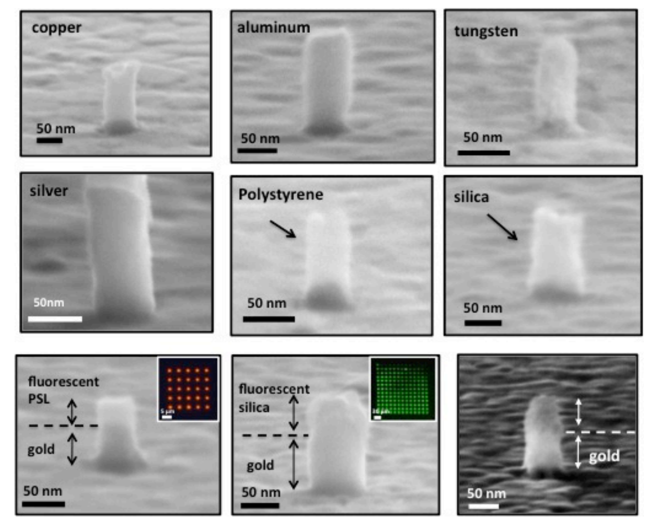
- All liquid-based processes, no chemical reactions, etching, or vacuum, and no toxic or aggressive chemicals.
- Feature size comparable to today's advanced electronics manufacturing technology at 20nm
- 10 – 100 times reduction in cost and 10 – 100 times faster throughput as compared with current technology
- 1000 times reduction in materials use compared to current technology eliminating 100s of process steps;
- Accelerate innovation with on-demand electronics.
- Crystalline metal and semiconducting structures at room temperatures.

Technology was funded by NSF (NSEC, NSF Award # 0832785), DoD and industry

Electrophoretic Directed Assembly– EPx Platform

Assembled Interconnects

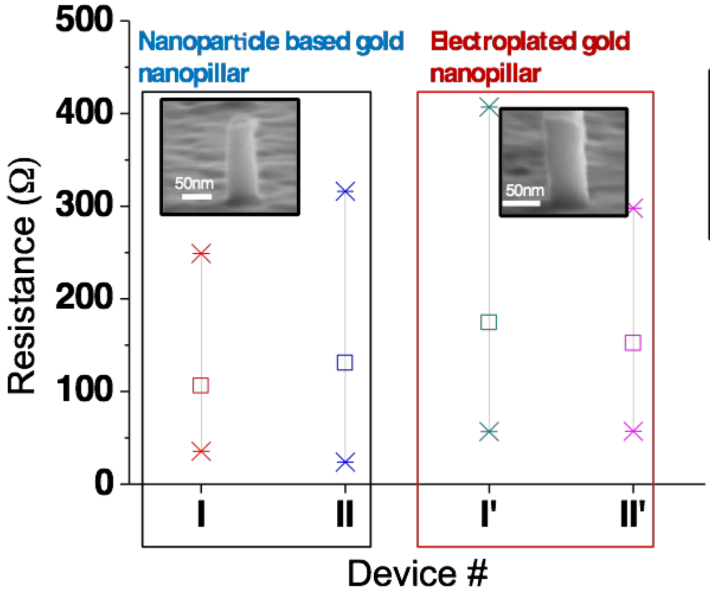


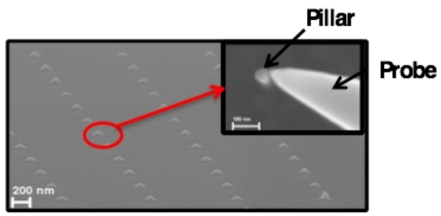


All assembled Nanoparticles are completely fused insitu.

ACS Nano, 8 (5), 2014.

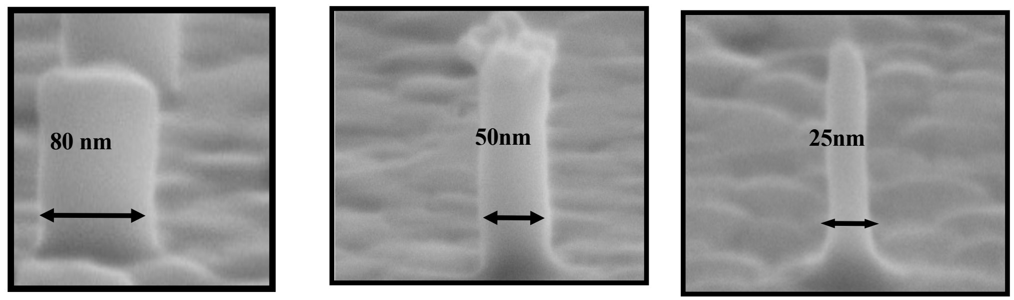
Interconnects Properties





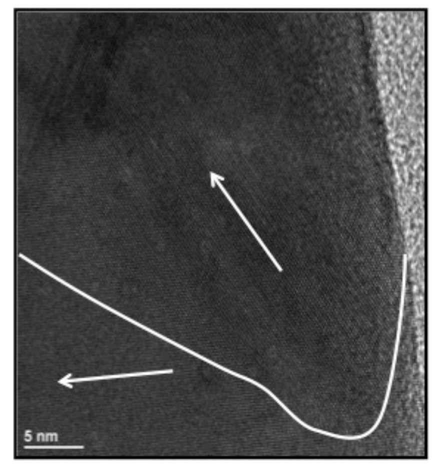
Resistance of assembled interconnects is the same as bulk (electroplated interconnects).

Crystalline Au Pillars



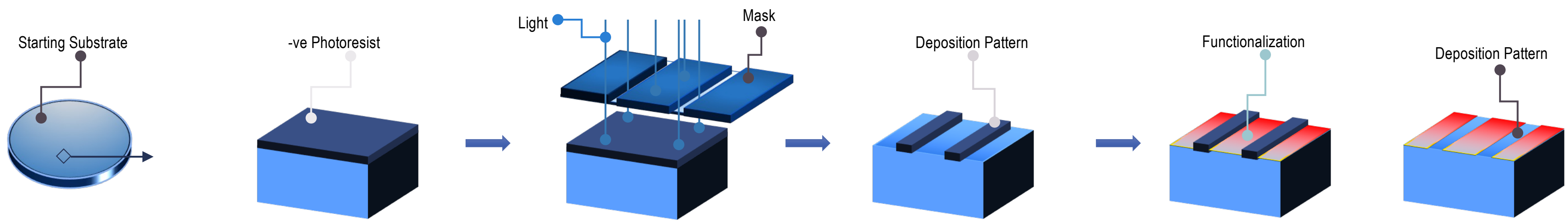
Directly assembled structures properties are equivalent to electroplating, CVD and PVD fabrication.

- TEM shows that NPs completely fuse without any voids at room temperature.
- Nanopillars have polycrystalline nature.



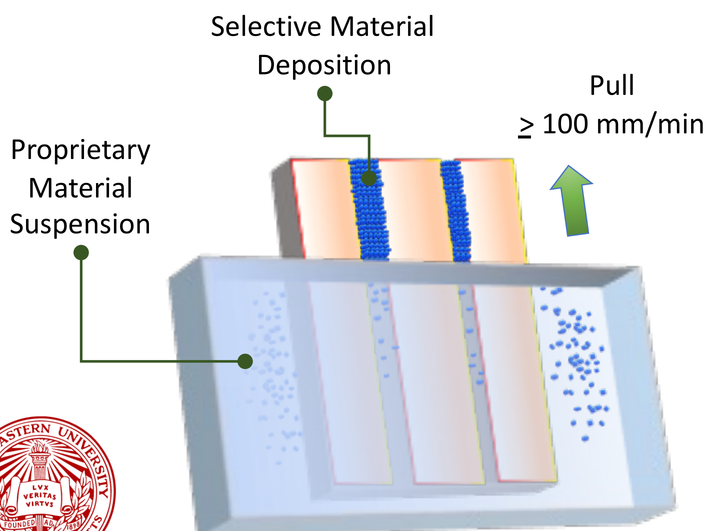
ACS Nano, 8 (5), 2014.

Fast Fluidic Assembly Process– FFx Platform

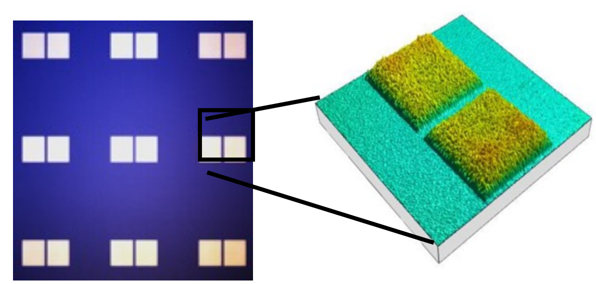


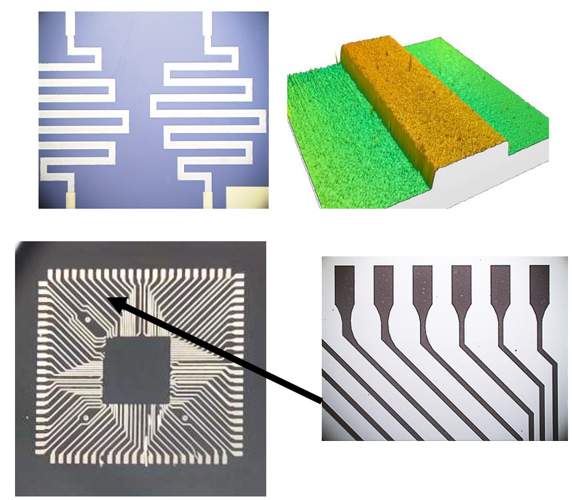
Patterning - Lithography

Functionalization



SiO_2 substrate – 10 µm spacing





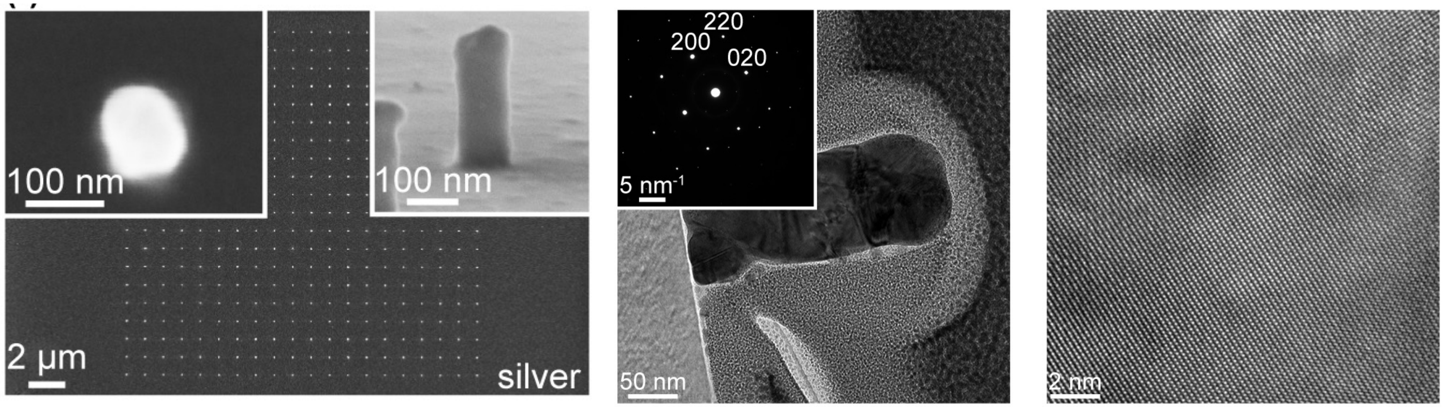
Fast Fluidic Assembly Process

ACS Nano 2022, October 21, 2022.

Additively manufactured electronics requires semiconductor, metal, and dielectrics.

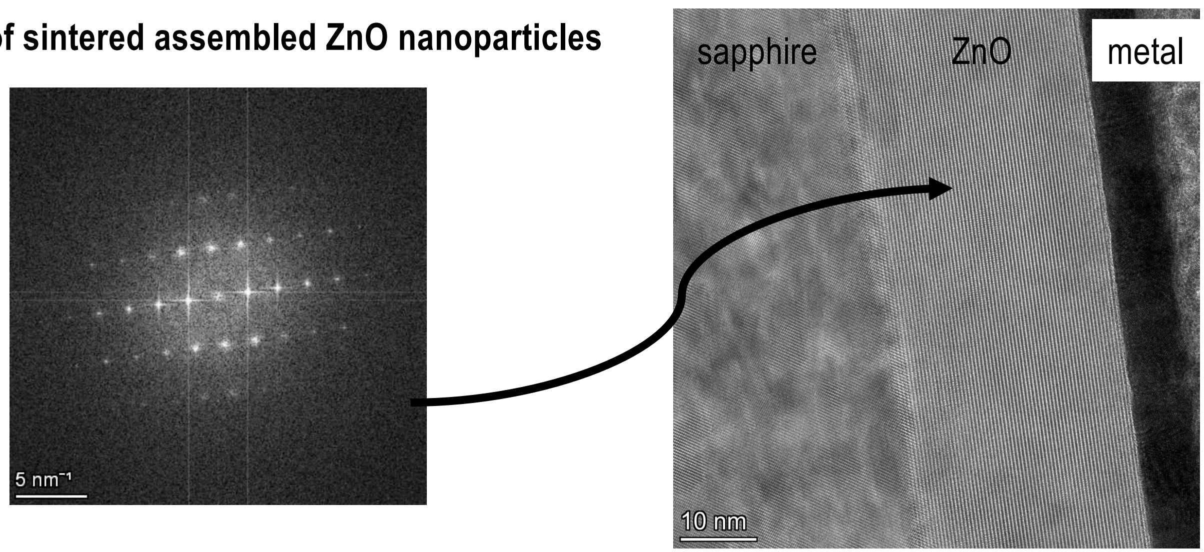
Additively Manufacturing Single Crystal Semiconductor and Metal

Advanced Materials, 2020.



Room temperature sintering to make single crystal metal (Ag) nano structures

TEM of sintered assembled ZnO nanoparticles



RTP sintering of II-VI nanoparticles (1000 c for 2 min) on sapphire yields gives a single crystal structure throughout.

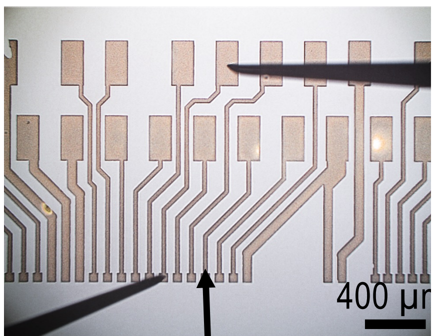
Additively Manufactured Metals Resistors, Fan out patterns, and Touch Display

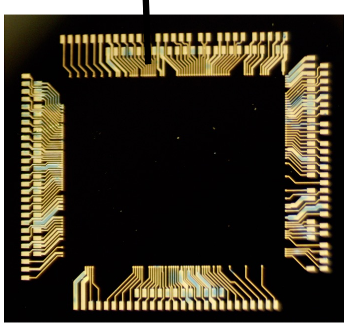
Additively Manufactured Metals Line

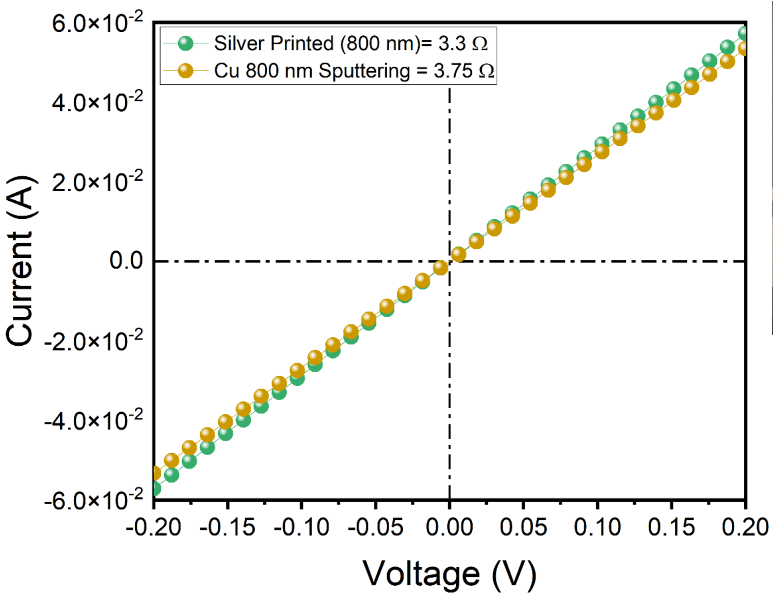
Silver vs Sputtered Copper

- Fan out Flip chip pattern was made using silver (internal pads < 40 microns)
- The trace's conductivity is equivalent to sputtered copper at the same thickness.

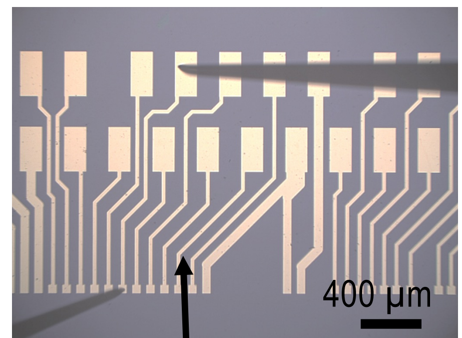
Silver

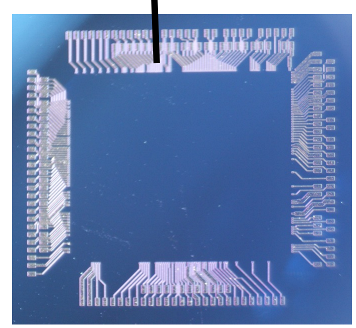


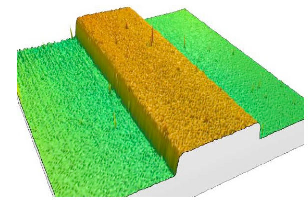


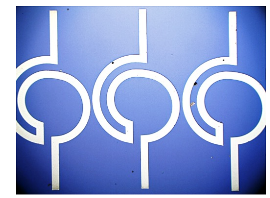


Copper (sputtered)

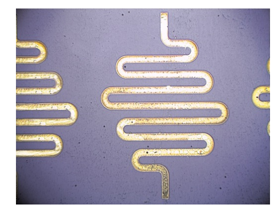




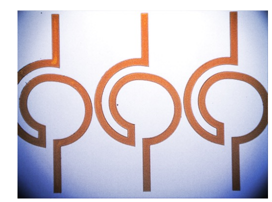




Platinum



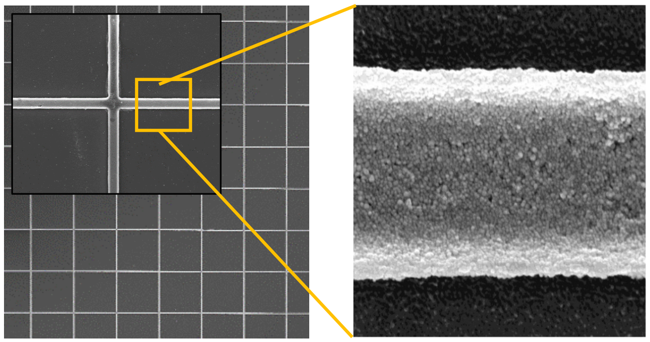
Gold



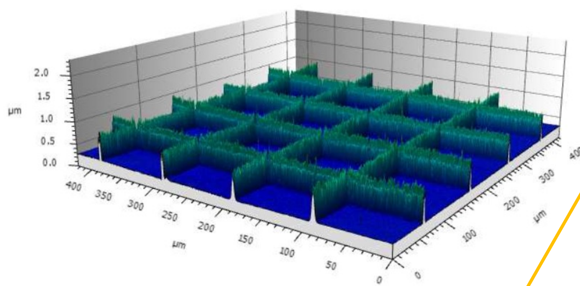
Copper

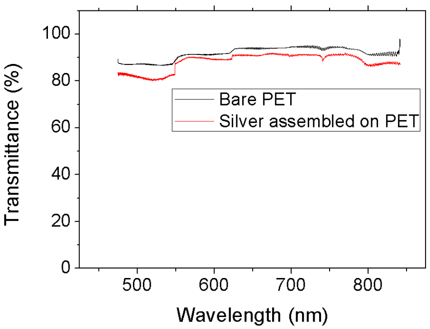
Additively Manufactured Touch Display at the Micro and Nanoscale

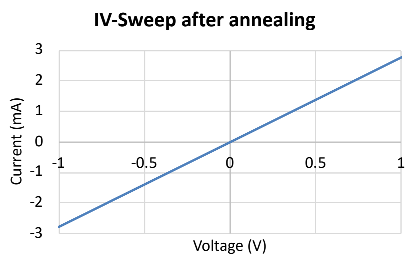
Ag grids for touch display applications

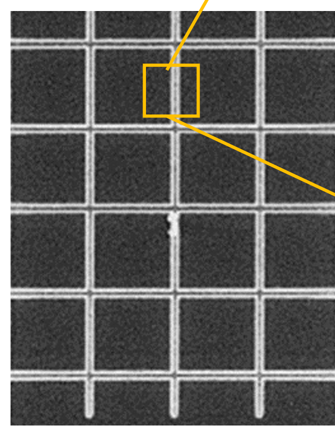


Line width 2 um

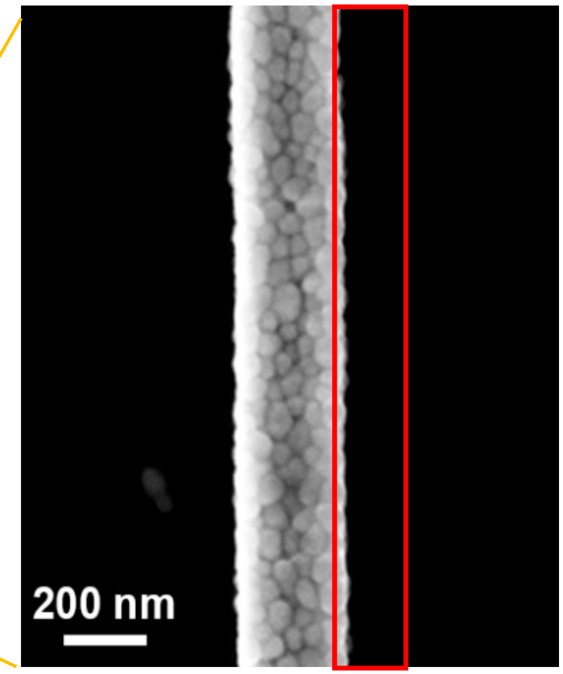








Line width 200 nm



Excellent Line edge roughness 3.7 nm
Using large nanoparticles

COMMUNICATION
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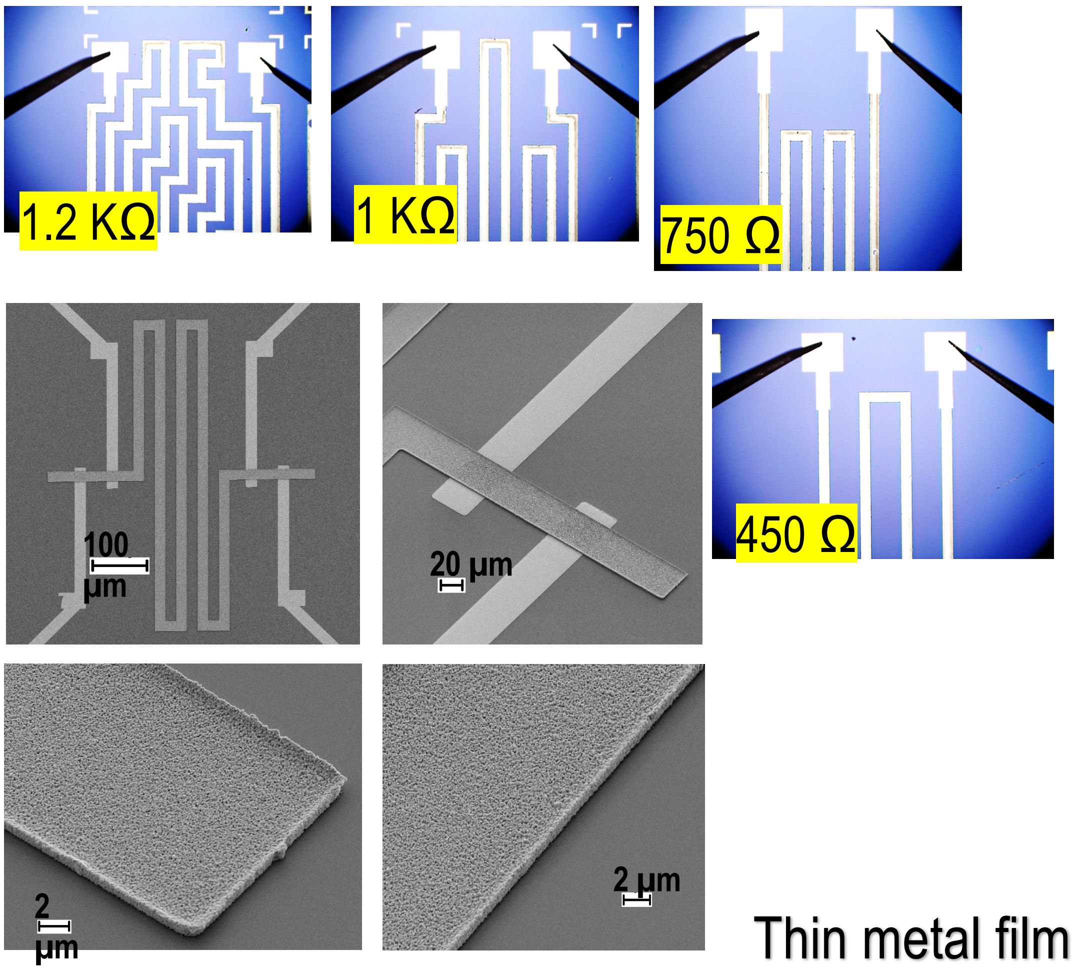
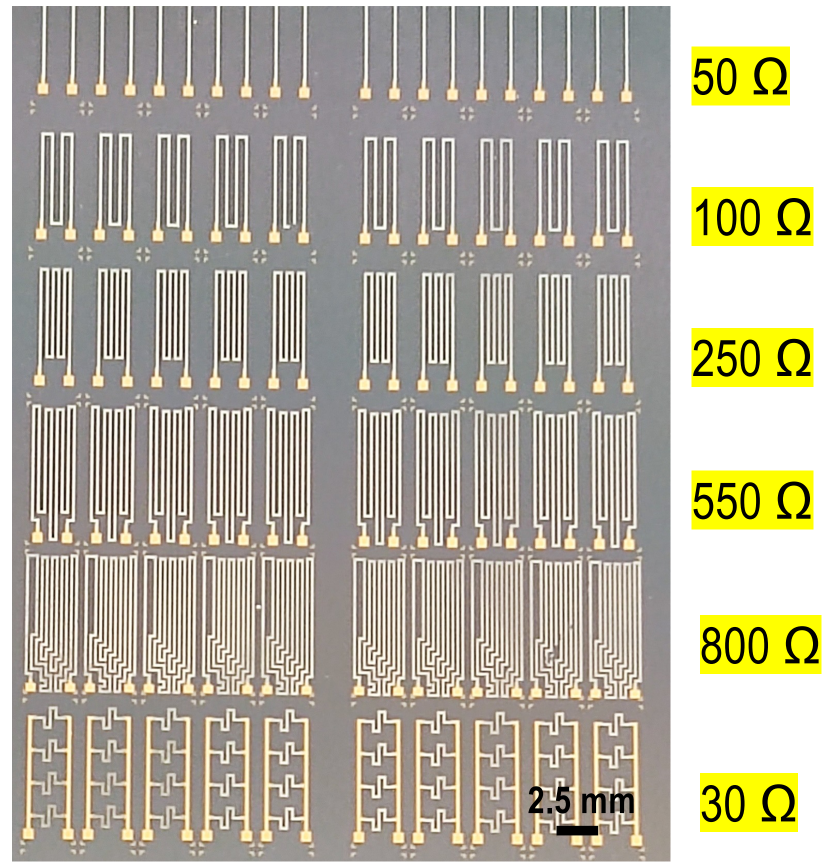
Scalable Printing of High-Resolution Flexible Transparent Grid Electrodes Using Directed Assembly of Silver Nanoparticles

*Salman A. Abbasi, Zhimin Chai, and Ahmed Busnaina**

Additively Manufactured Components: Resistors



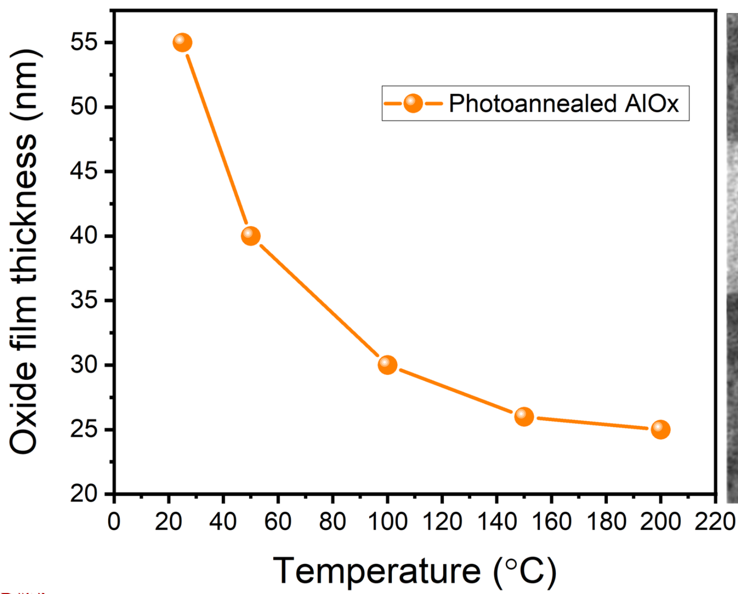


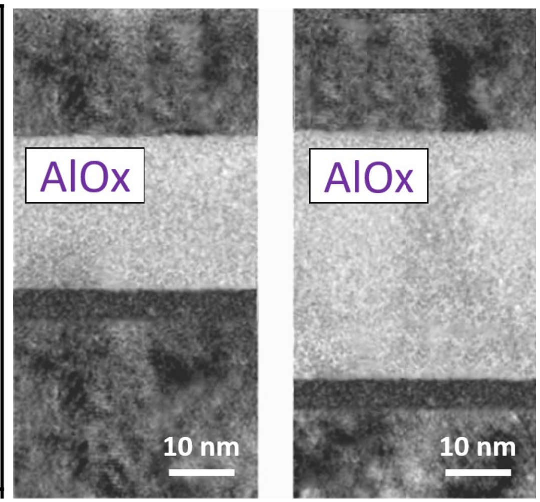
Thin metal film resistors

Additively Manufactured Dielectrics and Capacitors

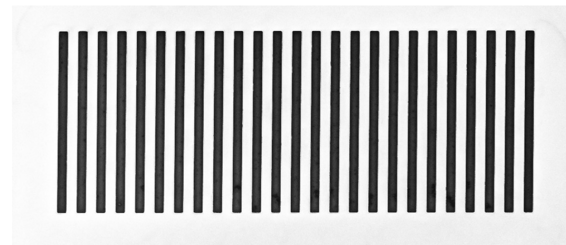
Characterization of Additively Manufactured Dielectric (Al_2O_3)

- The figure below shows the variation of the film thickness vs annealing temperature during the UV curing process with dielectric constant matching that of ALD deposited films ($\varepsilon_d = 7.2$).
- Higher temperature gives more densification and better dielectric as the TEM images show.

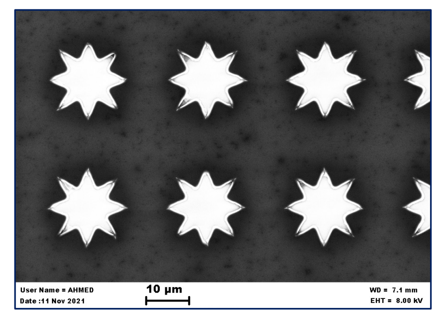




200 °C annealing 50 °C annealing

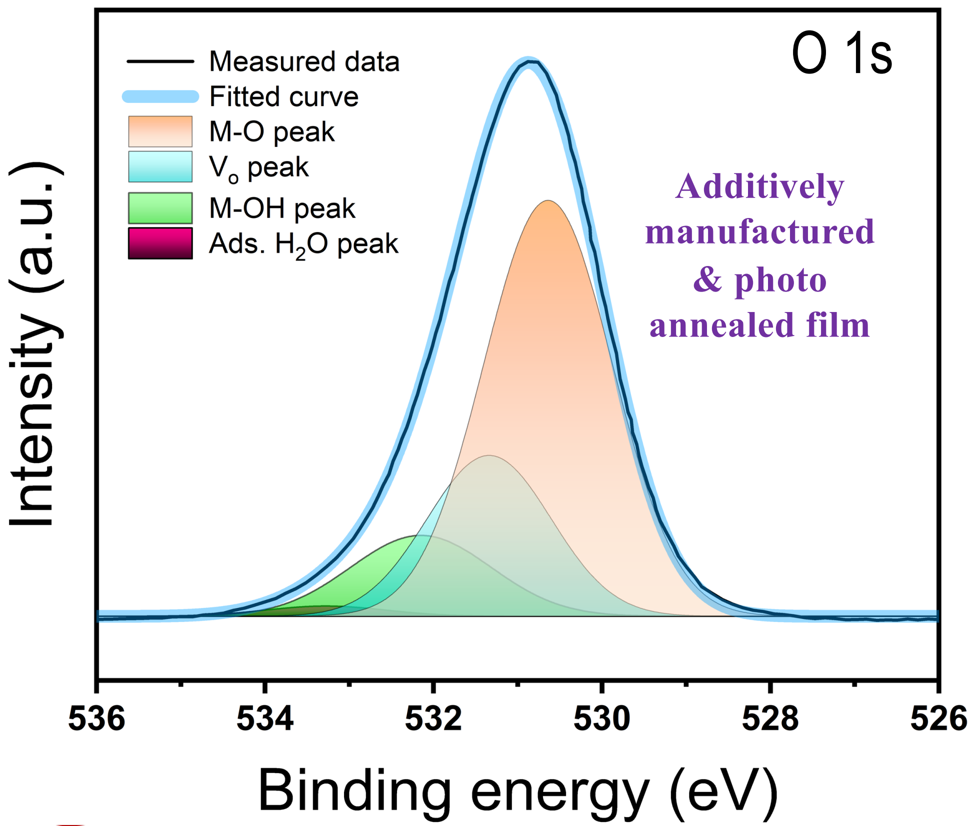


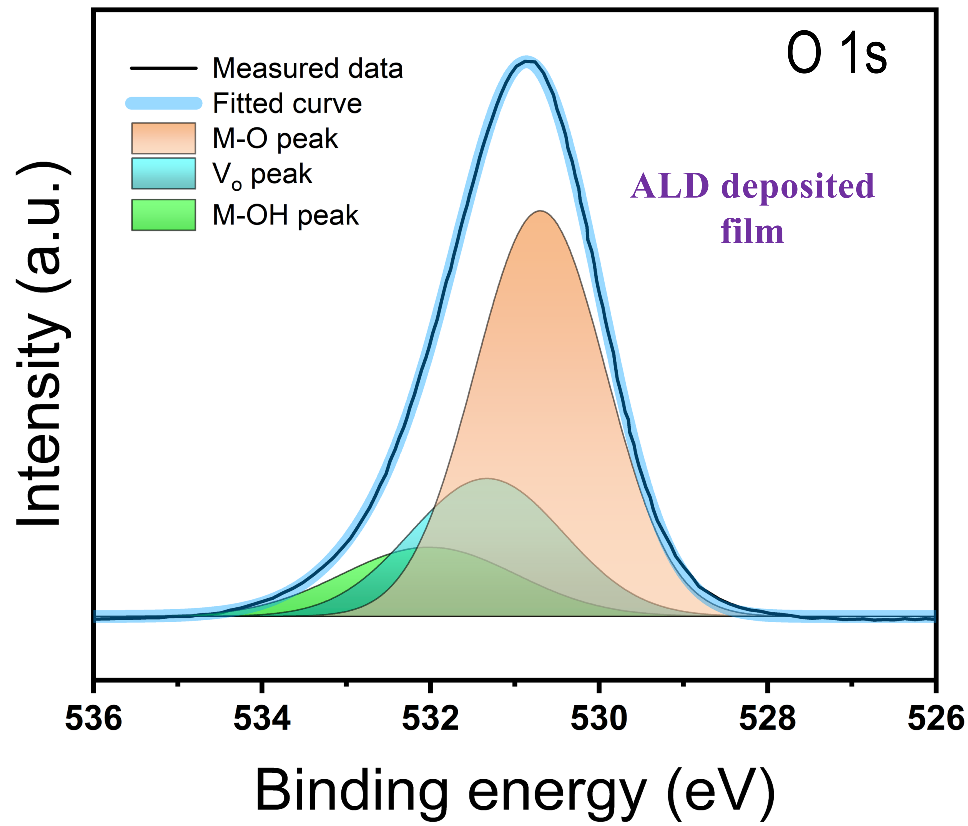
Dielectric channels
(10x200 microns and 50 nm thick)



X-ray Photoelectron Spectroscopy (XPS) Characterization of the Dielectric Layer

- The photo-annealed densified AlOx film is compared to a film deposited using ALD.
- We can observe large agreement in terms of peak intensities and composition ratios confirming the high purity of the oxide.

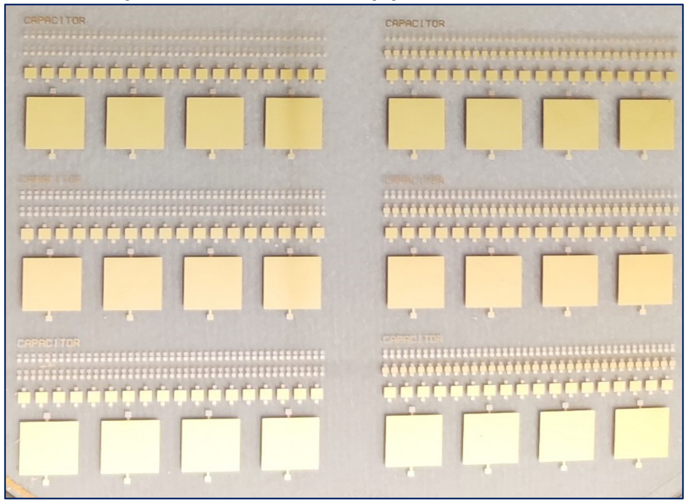




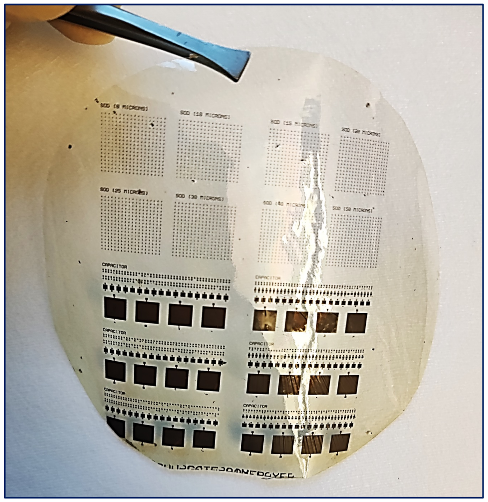
Additively Manufactured Capacitors on Rigid and Flexible Substrates

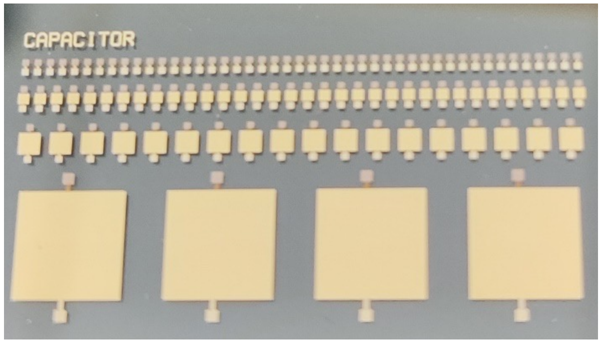
- Large-scale fabricated capacitors with a dielectric layer onto sapphire or polymer substrates.
- Each substrate has 640 capacitors with different surface areas of side lengths 20, 50, 100, 500, 1000, and 5000 µm.
- Metal: **Silver**
- Dielectrics: **Al_2O_3, SiO_2, HfO_2**

Capacitors on a sapphire substrate

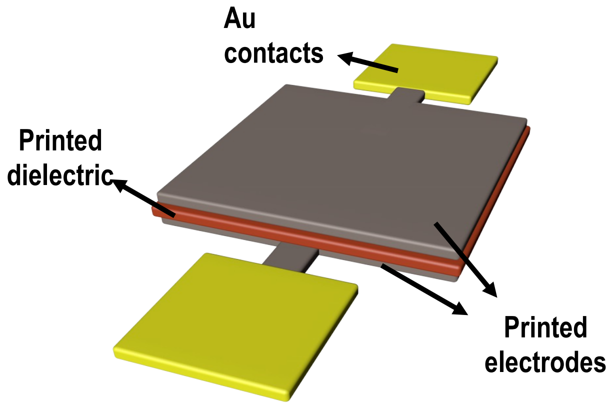


Capacitors on a polymer



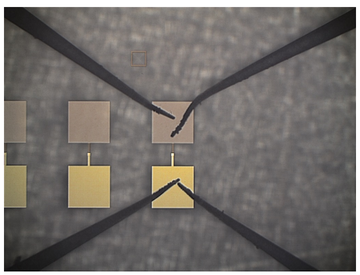


Capacitors on silicon



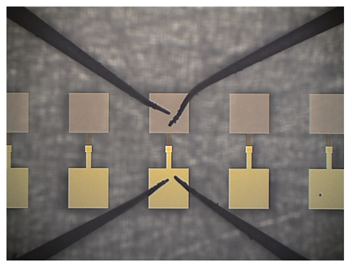
Characterization of Additively Manufactured Capacitors

- The capacitors need to show reliable performance under high frequency.
- The curve shows the capacitance variation versus different frequencies up to 1 MHz.



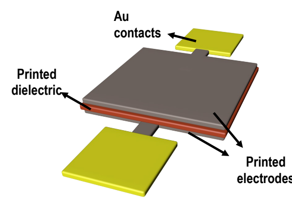
20x20 µm

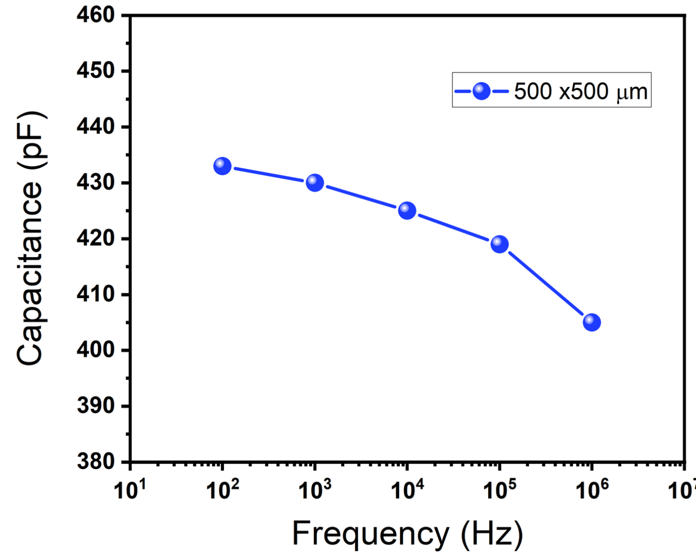
C= 857 fF

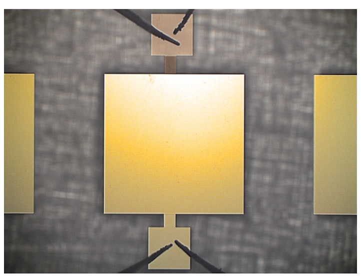


50x50 µm

C= 4.3 pF

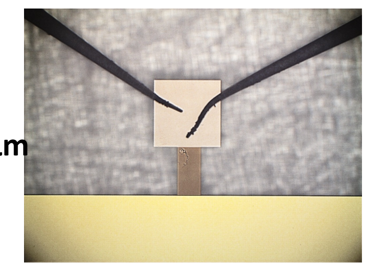






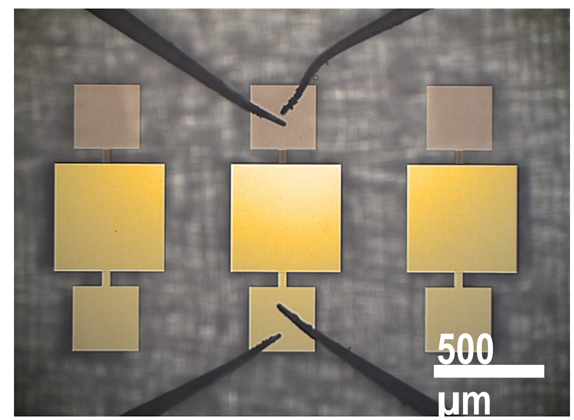
1000x1000 µm

C= 1.6 nF



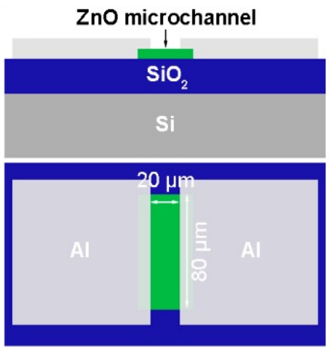
5000x5000 µm

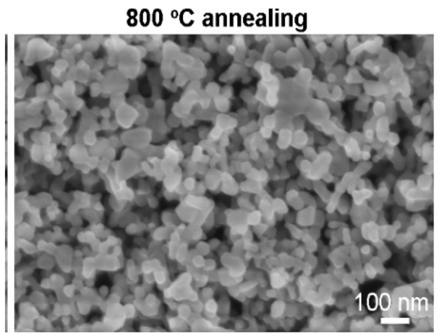
C= 5.68 nF

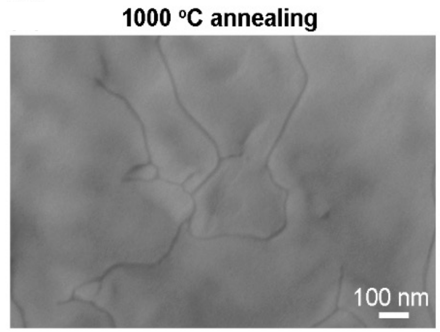


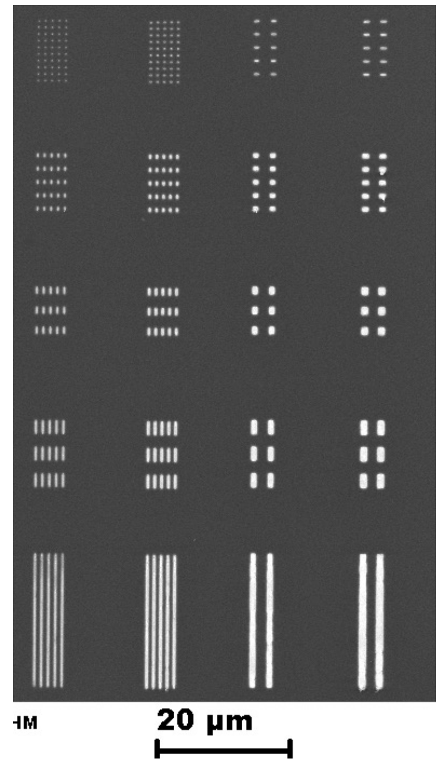
Additively Manufactured Active Components Transistors and Logic Gates.

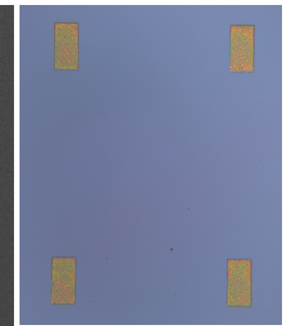
Field Effect Transistor Using II-VI Semiconductors



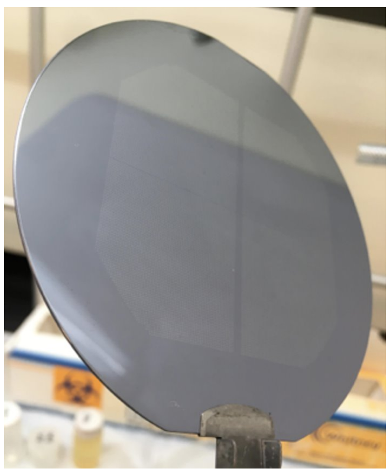


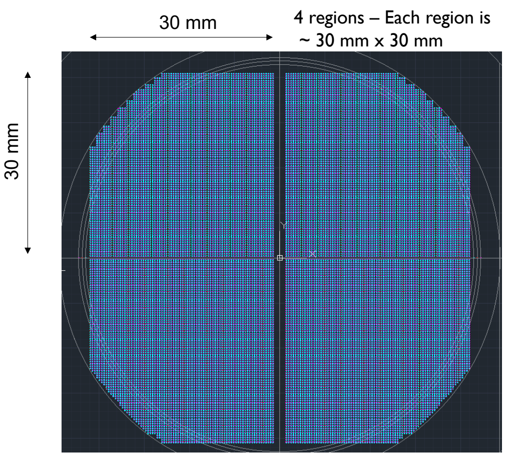


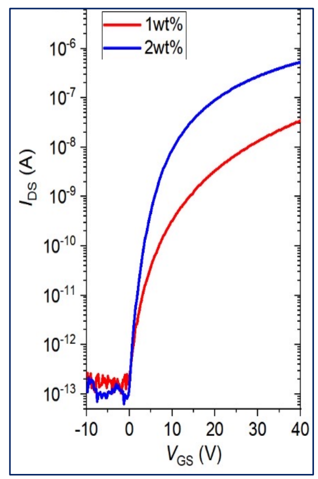




Channel width varied from 100 nm to 2 um, length varied from 100 nm to 20 um

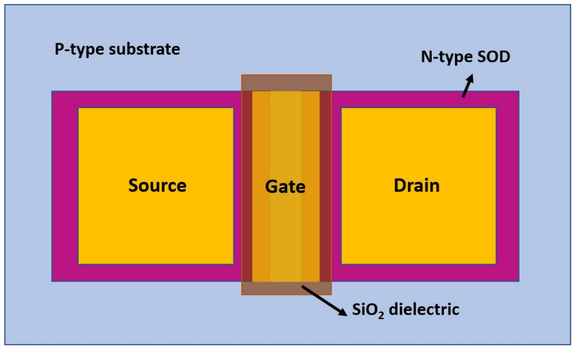


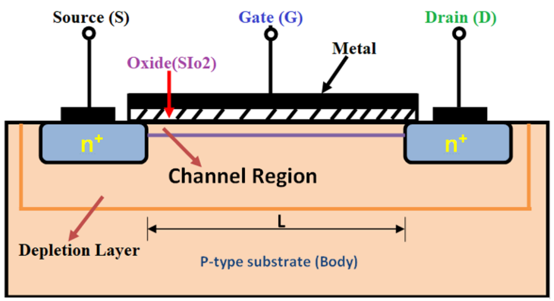




Wafer-level manufacturing of 37,000 transistors exhibiting an on/off ratio higher than 10^6 after annealing.

Additively Manufactured MOSFETs

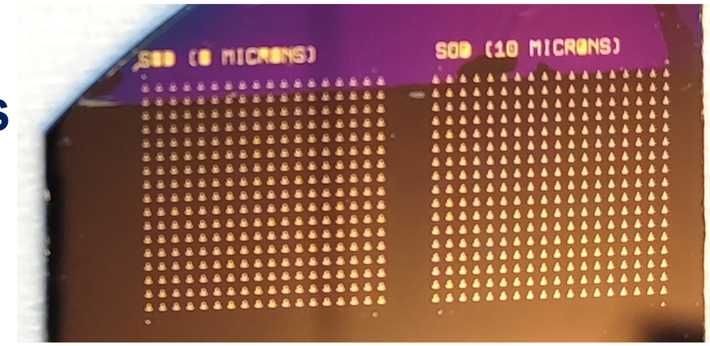


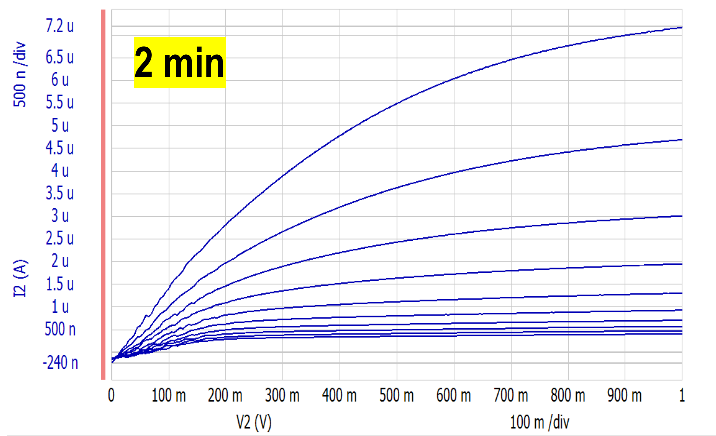


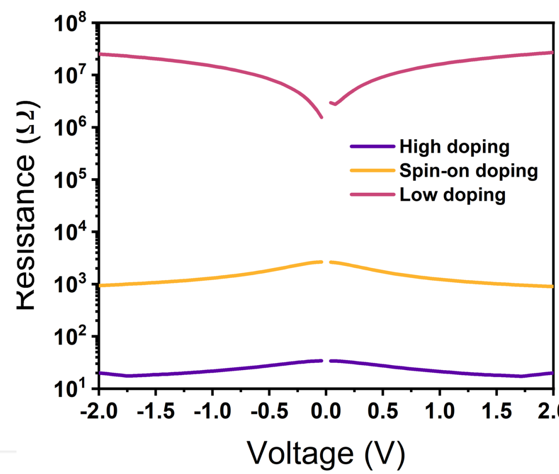
Metal: **silver,** Semiconductor: **silicon**

Dielectrics: **SiO_2,** Dopants: B+ and P-

A fully additive process to fabricate MOSFETs using dopants inks.

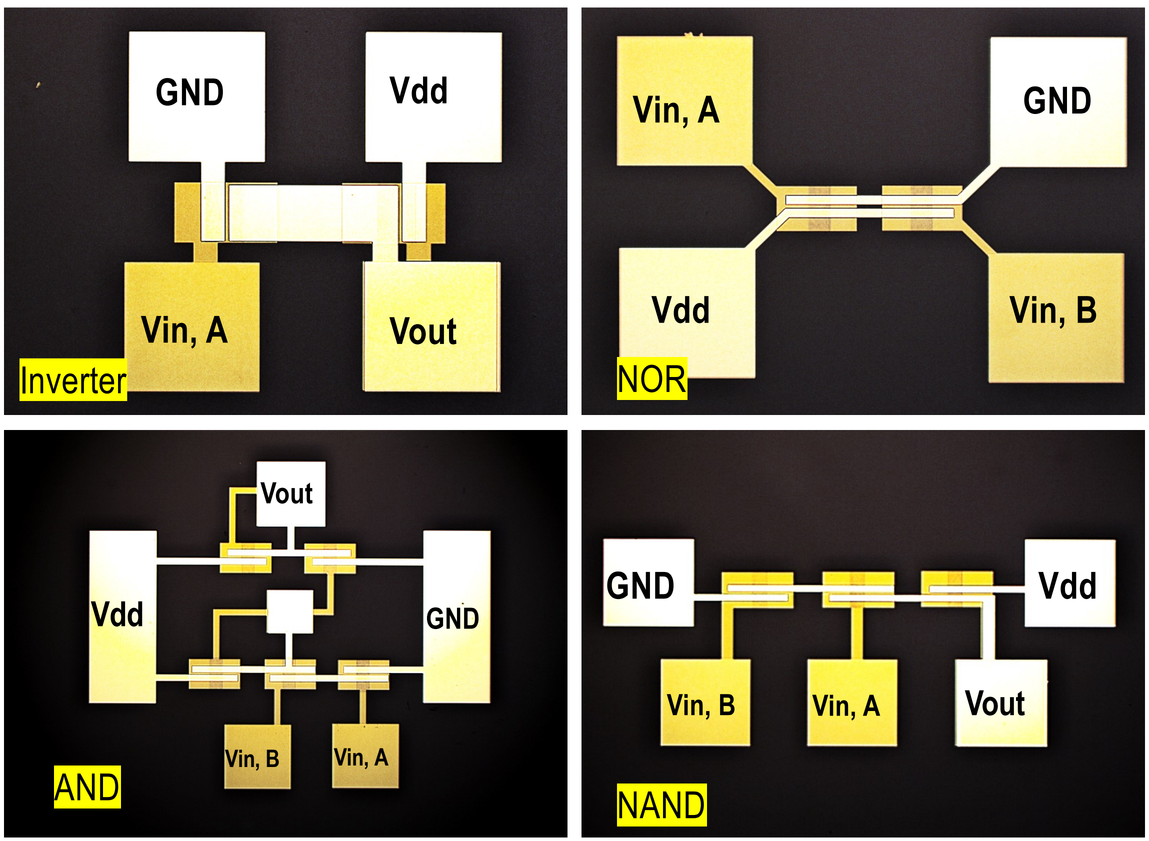


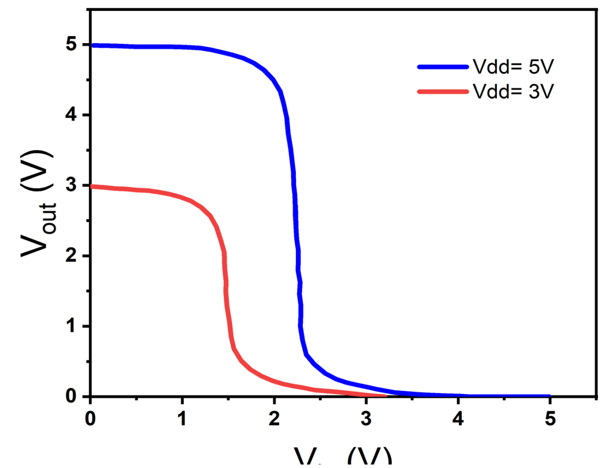


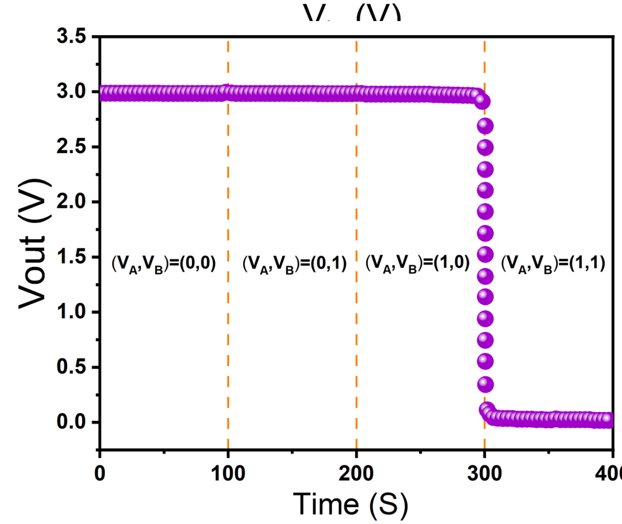


Additively Manufactured Logic Gate Electronics

- Logic gates such as Inverters, AND, NAND, and NOR were printed
- The figures below show the fabricated logic circuits.







Advanced Packaging for Heterogeneous Integration
for chiplet technology (integrating multiple dies in a package or system)

- **Conventional packaging approaches can not meet the resolution and density requirements. Presently, it can only be done at conventional fabs now.**
- **Additive manufacturing will enable lower costs, a faster development cycle**

NanoOPS

- **Submit DXF or GDS files and load ink, wafers, etc.**
- **Additively Manufacture:**
  - **micro and submicron interconnects.**
  - **passive and active components**
  - **onto silicon or substrates (interposers)**

Fully automated Additive manufacturing platform for electronics

Sustainable Additive Nanomanufacturing

- Comparing the embodied energy for making nanoscale transistors on a one cm^2 silicon substrate using directed assembly-based additive manufacturing and conventional fabrication show at least an **order of magnitude savings when using additive manufacturing**. (CIRP 2019)
- The new FFx platform, a fast fluidic assembly process, is estimated to **reduce the embodied energy cost by 20 times compared to conventional fabrication**.

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Procedia CIRP 80 (2019) 298–303

www.elsevier.com/locate/procedia

26th CIRP Life Cycle Engineering (LCE) Conference

Cumulative Energy Demand for Printing Nanoscale Electronics

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Conclusions

✓ Minimum feature demonstrated down to 25 nm and open material choices.

✓ 10 – 100x higher throughput and 1000x reduction in materials use.

✓ 10 – 100x reduction in manufacturing cost compared to current technology;

✓ More than 1000x faster than inkjet for on-demand electronics (one layer per minute).

✓ Capable of making crystalline metal and semiconducting structures.

Challenges:

- **Sintering to attain crystalline metal and semiconductor are still in the early stages of research and need much more research and development.**
- **Supply chain needed for nanoparticle suspensions (ink), especially copper.**

- **Our group had several research projects with Hanyang and Kookmin Universities on sustainable semiconductor manufacturing (CMP, Post CMP processes) and EUV lithography (funded by NSF/NRF and Intel).**
- **Unfunded collaborations were with PostTech, Busan, and Sungkyunkwan Universities.**

Acknowledgment

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To learn more: www.nano-ops.net