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The effect of hydrogen etching on 6H-SiC studied by temperature-dependent current-voltage and atomic force microscopy

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6H–SiC was etched with hydrogen at temperatures between 1000 and 1450 °C. The etched Si-terminated face for the 6H-SiC wafer was investigated by atomic force microscopy and temperature-dependent current–voltage ($I-V-T$) measurements. Mechanical polishing damage was effectively removed by hydrogen etching at temperatures above 1250 °C. Atomic force microscopy images revealed that very good surface morphology, atomic layer flatness, and large and large step width were achieved. Schottky diode characteristics were investigated in detail by current–voltage and temperature-dependent current–voltage measurements, and the results showed a transition from defect assisted tunneling to thermionic emission as the annealing temperature was increased from 1250 to 1450 °C. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1786632]

SiC, from the IV–IV group semiconductor family, has emerged as the leading candidate for high temperature and high power device applications due in part to the commercial availability of high quality SiC substrates of ever increasing diameter and quality. SiC is one of the first semiconductors discovered and its large cohesive energy caused some to mistake it for an element. Large Si–C bonding energy with short bond length leads to a large energy difference between bonding and antibonding states, resulting in wide band gaps. Low leakage current in SiC, many orders of magnitude less than that for Si, and reduced minority carrier generation rate, high breakdown electric field, high thermal conductivity, and high thermal stability are some advantages of SiC.

One of the main approaches for improving the yield of SiC devices is to reduce crystalline defects and achieve atomically flat surfaces, and minimize the formation of oxides. The preparation of the substrate surface is an important step in the technology of devices and low defect epitaxial films. To do so is especially difficult for SiC because of its mechanical hardness and chemical inertness. Although the standard polishing technique is a mechanical polish using diamond paste with decreasing grit sizes and results in a nearly specular surface on the macroscopic scale, microscopic morphology and subsurface damage still exists.[1,2] There are few methods such as hydrogen (H_2) etching, reactive ion etching, chemical mechanical polishing, and wet oxidation to remove scratches from the substrates. Among these techniques, high temperature H_2 annealing is the most commonly used since it can eliminate a large number of scratches arising from the polishing process and produces more ordered surface steps with full unit cell heights. In H_2 annealing, the SiC surface is exposed to hydrogen flow at temperatures of 1400–1700 °C.[3–10] Moreover, dangling bonds on SiC surfaces are terminated after etching with atomic hydrogen above 1100 °C.[11] Saidov *et al.* have shown that the character of SiC etching depends not only on the temperature and velocity of the gas flow, but on the heater as well.[12] Reports on the effect of annealing on defects in SiC have shown that one of two dominant deep levels at 0.36 eV anneals at 700 °C, which is suggested as a divacancy.[13] Other traps at 0.36 and 0.44 eV anneal at $T>1600$ °C. Traps can occur in pairs, residing on inequivalent lattice sites (cubic and hexagonal). Two overlapping intrinsic defects at 0.21 eV anneal at 600 °C.[14] One possible detriment of annealing may be degradation due to stacking fault formation at higher temperatures. There is the potential to introduce stacking faults if strain is present, since they have a low formation energy, and stacking fault formation energy in 6H-SiC is less than in 4H-SiC polytype.[15]

In our experiment, we have used inductively heated H_2 annealing to produce 6H-SiC surfaces suitable for Schottky devices. In order to examine the effect of the annealing temperature on the defects in 6H-SiC, the annealing temperature ranged from 1000 to 1450 °C with the annealing time remaining constant. The annealed surfaces at various temperatures were observed by contact mode atomic force microscopy (AFM). The fabricated Schottky diodes were characterized by current–voltage ($I-V$) and temperature–dependent $I-V$ ($I-V-T$) measurements.

Samples of n-type 6H-SiC wafers with carrier concentration of $2\times10^{18}/\mathrm{cm}^3$ obtained from Cree Research Inc. were diced into 10 mm × 10 mm and chemically cleaned in boiling trichloroethlene, acetone, and methanol for 5 min in each solvent, then rinsed with de-ionized water for at least 30 s and dried with flowing nitrogen. The cleaned samples were dipped into a 10:1 HF solution for 30 s to remove the grown silicon oxide from the surface, rinsed with water and dried with nitrogen again. For etching studies, the samples were mounted on a SiC coated graphite and loaded in a water-cooled quartz tube. Three different annealing conditions (1000, 1250, and 1450 °C) were used to anneal the Si-terminated face of samples for 30 min in flowing hydrogen. The temperature of the SiC wafer was monitored using an optical pyrometer with the emissivity set at 0.7. The temperature of the system was also calibrated by two different

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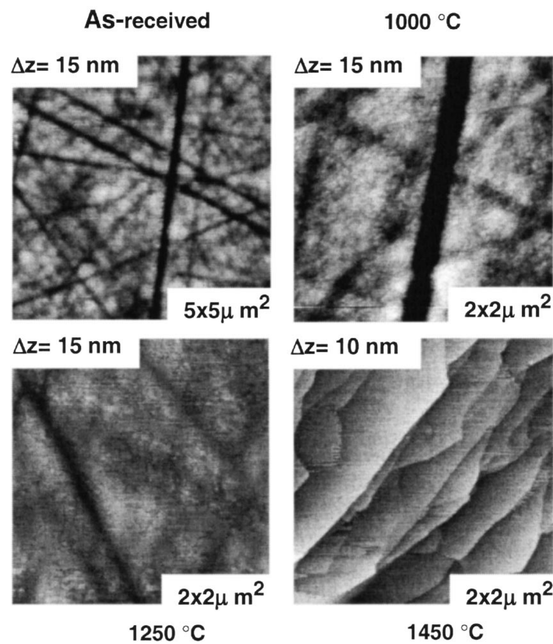

FIG. 1. AFM images of the as-received 6H-SiC wafer having high density of scratches on the surface, and annealed at 1000, 1250, and 1450 °C for 30 min.

means, i.e., by the melting point of Ag, and by type C thermocouple (W/Re). Ni/Ti/Au (500 Å/300 Å/750 Å) metallization was deposited using electron beam (Ti and Ni) and thermal evaporation (Au) in order to form ohmic contacts and the contacts were annealed at 950 °C for 2 min by rapid thermal annealing in nitrogen ambient. Ni/Au (300 Å/750 Å) metallization was then used to form Schottky contact through shadow mask. Schottky contacts on the samples were 500 μm in diameter. The current for $I-V-T$ measurements was collected using an HP 4140B picoammeter. The measurement temperature ranged from 80 to 700 K, with <1 K stability at each temperature step.

Figure 1 shows the effect of hydrogen annealing to the 6H-SiC wafer. The as-received 6H-SiC substrates showed a large number of deep and irregularly directed scratches over the entire surface. After annealing at 1000 °C for 30 min, the scratches diminished but did not vanish completely. When the annealing temperature was increased to 1250 °C, the AFM images revealed that the surfaces became very flat. Importantly, annealing at 1450 °C for 30 min resulted in atomic layer flatness, and the surface morphology showed atomic terraces and steps. These terraces are due to a small misorientation of the surface with respect to the exact (0001) basal plane. The step height for the 6H-SiC should be six-paired atomic monolayers corresponding to about 1.52 nm, which is in agreement with the experimental observations (1.60 nm).[16] The surface roughness (rms value) measured from the area shown is 0.58 nm, which is low enough for device applications. The $I-V$ properties also showed successive improvement with anneal temperature. Better $I-V$ results were obtained at higher annealing temperatures. As can be seen in Fig. 2, the leakage current decreased by more than two orders of magnitude as the annealing temperature increased from 1000 to 1450 °C.

The $I-V-T$ for each annealing temperature showed high and relatively temperature-insensitive current, resulting in a curved Arrhenius plot of current at various reverse bias conditions versus 1/kT. Figures 3(a) and 3(b) show the $I-V-T$ for the sample annealed at 1250 and 1450 °C. The energy at high temperature, measured as the slope, decreased with increasing reverse bias. Energy versus $V_r^{1/2}$ from $I-V-T$ was linear, consistent with either thermionic-field emission or a Poole–Frenkel effect acting on a donor defect.[17] Extrapolation of energy to zero bias gave an energy of 1.25 eV above the Schottky metal energy level. $C-V$ measurements gave a Schottky barrier height of 1.3 eV, consistent with the barrier energy from $I-V-T$ measurements. Similar measurements for the sample annealed at 1000 and 1250 °C gave extrapolated energies of only 0.495 and 0.335 eV, respectively, pre-

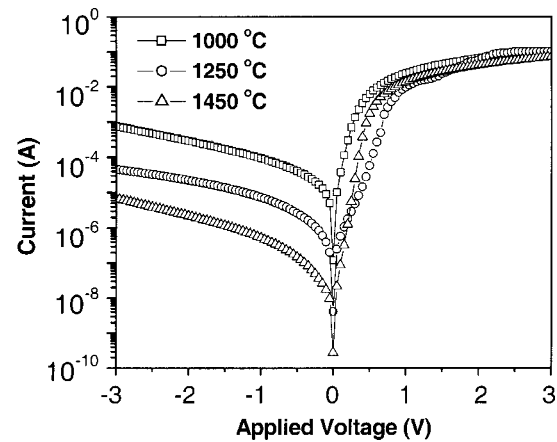

FIG. 2. $I-V$ behavior of hydrogen etched SiC substrates annealed at different temperatures for 30 min.

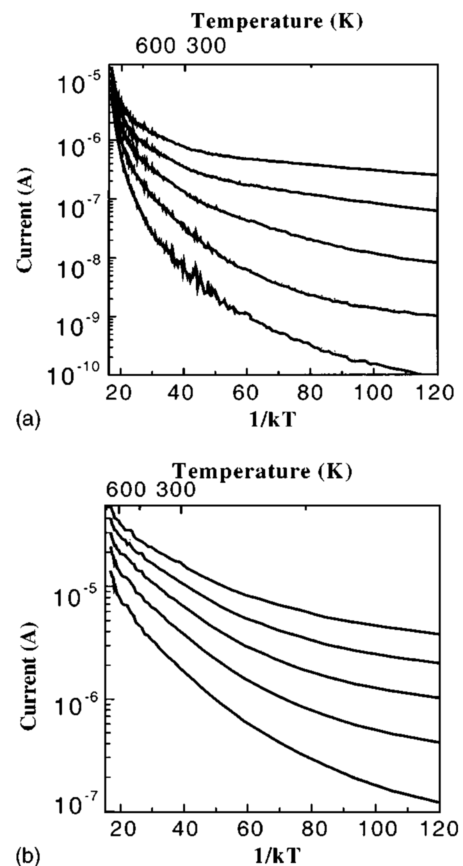

FIG. 3. $I-V-T$ measurements for 6H-SiC annealed in hydrogen at (a) 1450 °C, and (b) 1250 °C. Voltages ranged from –1 V (bottom) to –3 V (top) in 0.5 V steps.

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sumably due to tunneling mediated by interface defects. Plots of IdV/dI versus current[18] at 300 K showed that the ideality factors decreased from 2.44 and 2.58 for annealing temperatures of 1000 and 1250 °C, respectively, to 1.44 for the SiC annealed at 1450 °C. Ideality factors near two indicate defect mediated conduction, while ideality factors of one indicate ideal thermionic emission conduction. Ideality factors over two indicate a shunting term, such as by tunneling conduction. A Richardson plot at a forward bias of 0.5 V for the sample annealed at 1450 °C showed two distinct slopes with energies of 0.347 eV up to 350 K, and 1.15 eV above 350 K. The lower energy corresponds to the energy of one of the dominant defects at 0.36 eV that has been shown to survive annealing at $T > 1600$ °C.[13] The higher energy corresponds roughly to the barrier height, which compares reasonably well to 1.25 eV from $I-V-T$ and 1.3 eV from $C-V$.

This work showed that significantly improved $I-V$ behavior ensued when 6H-SiC annealing temperature was raised from 1250 to 1450 °C. This is also the range of temperatures where AFM images showed a shift in surface morphology to distinct steps. Clearly, this annealing temperature range reduces the concentration of low energy defects responsible for trap assisted tunneling, reducing the reverse bias leakage current by two orders of magnitude compared to samples annealed at 1000 °C, and by one order of magnitude compared to samples annealed at 1250 °C. Further experiments are intended to anneal at higher temperatures to see the effect of annealing on the Schottky diodes after modification of the annealing chamber.

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